TEL AVIV UNIVERSITY

THE IBY AND ALADAR FLEISCHMAN FACULTY OF ENGINEERING

The Zandman-Slaner Graduate School of Engineering

Vertical Junction Si Cells For Concentrating Photovoltaics

By

Roni Pozner

THESIS SUBMITTED FOR THE DEGREE OF "MASTER OF SCIENCE" IN MATERIALS SCIENCE AND ENGINEERING

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This research was carried out in the School of Electrical Engineering Department of Physical Electronics under the supervision of Prof. Yossi Rosenwaks

October 2010

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Abstract

Vertical Junction (VJ) Si cell have shown potential to operate at high concentration, mainly the result of reduced series resistance losses due to the low current/high voltage design, but tests and analysis have shown so far only modest efficiency of about 20%. We perform a comprehensive optimization study and show that the conversion efficiency of VJ can be significantly larger, close to 30% at concentration of 1000. Reaching this efficiency requires junction dimensions that are significantly smaller than past VJs. This may require a different approach to the fabrication process, possibly using a monolithic method rather than the wafer stacking approach. We also show that a major contribution to the outstanding performance of the VJ at high concentration is the increased photoconductivity effect, which is usually negligible in conventional cells, but produces a significant reduction in series resistance of the VJ when illuminated at high concentration.

Dense-array VJ modules with high-voltage cells should allow a parallel connection with voltage matching rather than series connection with current matching, leading to lower mismatch losses under non-uniform illumination. However, the module-level performance of a VJ dense array under non-uniform illumination has not been studied. We present the performance of a module comprising VMJ cells connected in parallel, compared to a conventional module with cells connected in series. The number of junctions in a single VMJ cell is a free parameter for optimization. The results show a clear advantage of the VMJ module over the conventional module under non-uniform flux, allowing reduction or even elimination of homogenizing secondary optics.

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List of Symbols

Symbol	Description
J_{sc}	Short-circuit current
q	Electron charge
η_a	Absorption efficiency
λ	Wavelength
C	Concentration ratio
Z	Junction depth
η_{coll}	Collection efficiency
W	Junction width
N	Sun Intensity or Number of vertical junction in a VMJ cell
τ	SRH lifetime
τ_{max}	SRH lifetime of the intrinsic FZ silicon substrate
V_{oc}	Open circuit voltage
H	Junction depth or Homogenizer length
p	Holes concentration
n	Electron concentration
μ_n	Electron mobility
μ_p	Hole mobility
T	Transitivity
R	Reflectivity
n	Refraction index or Ideally factor
e	Exponent
α	Absorption coefficient
σ	Conductivity
R_S	Series resistance
R_P	Shunt resistance
V	Electric potential
ρ	Resistivity

I	Current
I_{ph}	Photon generated current
I_s	Saturation current
J	Current flux
E	Electric field
k	Boltzmann's constant
T	Absolute temperature
ε_0	Dielectric permittivity of vacuum
ε_{Si}	Dielectric permittivity of Si

List of Abbreviations

AR	Aspect ratio
ARC	Anti reflective coating
BSR	Back surface recombination
CPV	Concentrating PV
DC	Direct current
DRAM	Dynamic random access memory
DRIE	Deep Reactive Ion Etching
FF	Fill factor
FSR	Front surface recombination
FZ	Float zone
IV	Current-Voltage
K_2CO_3	Potassium carbonate
MCE	Metal Coverage Ratio
MEMS	Micro-electromechanical systems
MIM	Monolithic Integrated Modules
PECVD	Plasma-enhanced chemical vapor deposition
PV	Photovoltaic
PVD	Physical vapor deposition

RC	Reflective coating
Si	Silicon
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
SRH	Shockley-Read-Hall
SOI	Silicon on insulator
VJ	Vertical junction
VMJ	Vertical multi junction
TCAD	Technology computer aided design

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Introduction

Silicon high-voltage Vertical Multi-Junction (VMJ) or edge-illuminated cells have been proposed since the 1970's [1]. Each VMJ cell consists of several VJs connected in series. An ideal VJ structure possesses several inherent advantages over conventional PV cells. First, such a structure allows decoupling of the photon absorption and carrier collection axes allowing more degrees of freedom for optimization compared to conventional horizontal junctions. Second, since the current flow in this device is mostly lateral, the series resistance losses in the emitter region and electrodes are negligible. As a result, a VJ device shows high conversion efficiency under very high flux concentration [2]. The trade-off between front contact grid shading and series resistance, encountered in conventional concentrator cells [3] is also avoided in the VJ.

High-voltage cells with low series resistance can be good candidates for concentrating PV (CPV) systems, that are usually constrained by high currents leading to high losses related to series resistance. Additional applications where high voltage, high efficiency, small area cells can be a good choice include solar-powered stand-alone smart systems such as wireless sensor network [4], or micro electromechanical (MEMS) devices [5].

High-voltage VMJ cells have been produced in the past by stacking multiple wafers followed by orthogonal cutting, and have shown capability to accept high concentration of up to 2,500 suns, with peak efficiency of about 20% [2]. Similar VMJ cells, developed for low concentration of (20-50) suns, were reported with lower efficiencies of around 15% [6]. An alternative high-voltage cell design is the Monolithic Interconnected Module (MIM), based on segmenting a conventional horizontal silicon junction and adding a series connection using top-to-bottom electrical contacts [7,8]. Although high output voltage was achieved in these MIM designs, reported conversion efficiencies in Si are lower than 12%, making them unsuitable for CPV systems.

If the VJs in a VMJ cell are manufactured monolithically on a single wafer, rather than by stacking of multiple wafers, then the width of each junction can be varied independently of the wafer thickness. The junction geometry, as well as doping

profiles, surface treatments, etc., can be optimized with greater freedom compared to the approach of [2] and [9]. This then presents a comprehensive analysis and optimization of a monolithically designed VMJ cell, taking into account a wide range of design parameters and concentration levels.

Non-uniform illumination is a known problem in high-concentration dense-array photovoltaic systems. Under such circumstances, series connection of cells in the array will result in current mismatch leading to severe degradation in system performance. This is less of an issue in single optic/single cell systems, as long as all optical units are reasonably well aligned and produce the same illumination for each cell. In dense array systems, a known solution is to use an optical flux homogenizer [19]. Although such a device can meet the flux homogeneity requirements, the introduction of an additional optical device will inflict additional losses, which can reach 10% or more for typical designs [20], as well as additional cost and complexity.

PV cells with high voltage and low current can be connected in parallel rather than in series and still provide a reasonably high output voltage of the module. This leads to voltage matching rather than current matching within the module. Since cell voltage is less sensitive to illumination, voltage matching should produce lower performance degradation under non-uniform illumination, compared to the series connection used in conventional dense array modules.

In this work we consider a module made of VMJ cells under non-uniform concentrated illumination produced by a dish concentrator with a reflective homogenizer. The performance of this module, and in particular the loss attributed to electrical mismatch between the cells, is compared to the performance of a module made from conventional cells connected in series under the same incident radiation distribution.

Research goals

This research proposes to develop a novel photovoltaic cell converting sunlight to electricity at higher efficiency relative to existing cells. The improved cell has better flexibility for integration in modules, both one-sun and concentrating.

The new cells contain many small sub-cells, which are internally connected in series. Such configurations are usually called Monolithic Integrated Modules (MIM) and they are capable of providing very high open circuit voltage. We propose to develop and demonstrate a new MIM design principle based on a monolithic device with VJs offering significant expected advantages in performance relative to existing MIM designs. The advantages include higher voltage, lower series resistance, less shading, and better matching to integration in modules including concentrator modules.

The thesis will address the following issues:

1) Produce a quantitative estimate of the expected advantages of the VJ based on modeling and simulation of the physical model.

2) Modeling the series resistance and high concentration behavior of the VJ.

3) Define materials and manufacturing processes that can make the new design practical.

4) Construct and test prototype cells to validate the newly designed manufacturing procedure, performance estimates and temperature resilience.

5) Analysis of module and system level aspects such as low sensitivity to non-uniformities of the incident concentrated flux, low sensitivity to partly shading conditions and the voltage-coupled connection instead of the traditional current-coupled approach.

1 Literature Review

High-voltage VMJ cells have been produced by stacking multiple wafers followed by orthogonal cutting, and have shown capability to accept high concentration of up to 2,500 suns (Figure 1), with peak efficiency of about 20% [2].

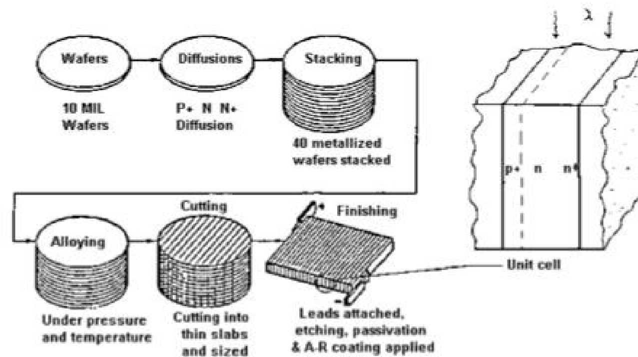


Figure 1: Sater & Sater, 29 IEEE PV Specialists Conference, 2002

Similar VMJ cells, developed for low concentration of (20—50) suns, were reported with lower efficiencies of around 15% (Figure 2) [6].

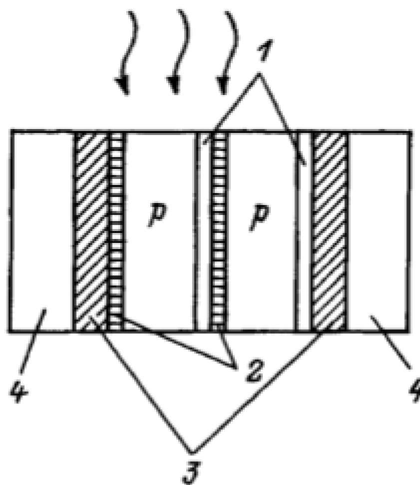


Figure 2: Structures of silicon solar cells with vertical p–n junctions produced by diffusion welding and direct bonding: 1 - p^+ layer, 2 - n^+ layer, 3 - Silumin, 4 - heat compensator.

An alternative high-voltage cell design is the Monolithic Interconnected Module (MIM), based on segmenting a conventional horizontal silicon junction and adding a series connection using top-to-bottom electrical contacts (Figure 3) [7,8]. Although

high output voltage was achieved in these MIM designs, reported conversion efficiencies in Si are lower than 12%, making them unsuitable for CPV systems.

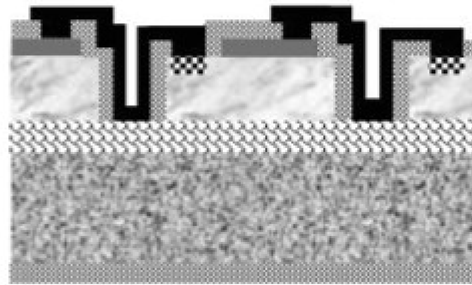


Figure 3: High Voltage Photovoltaic Mini-modules

Detailed analyses of VMJ junctions and cells are available in [9] but they address large junction width in the range of 300—1,000 µm and low concentration of up to only 10 suns. The Sliver cell (Figure 4) described in [10] seems like a VJ, since the electrical contacts are placed at the side edges. However, in the Sliver cell most of the photogenerated electrons first flow towards the diffusion layers at the top and bottom surfaces of the cell, and then flow sideways towards the contacts. Correspondingly, the series resistance reported in [10] is mostly the sheet resistance at the emitter layers just as in conventional cells. For this reason, the Sliver cell cannot be considered as a true vertical junction cell.

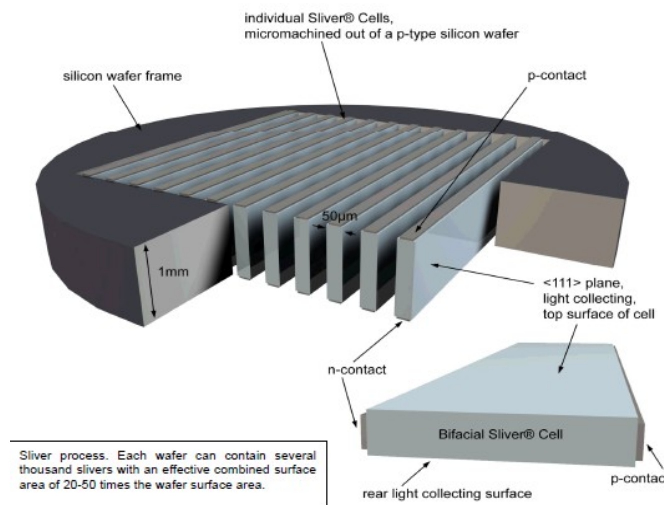


Figure 4: A wafer containing Sliver cells. The p–n junction is located below each of the large, light-collecting surfaces

An analysis for VMJ cells under high concentration up to 2,500 was reported by Rafat in [11], but it was based on an approximate analytical model, and it was limited

in the range of design parameters. For example, in all the practical simulations, the junction width was defined as the thickness of the wafers used by Sater in [2]. Hence, it was limited to the thickness of practically manufactured wafers. Although the performance of an ideal cell is analyzed under a wide range of concentration levels, the optimization for cells with real parameters was conducted only for 1 sun. Rafat concludes his work with the call for a thorough numerical analysis of the VJ under high concentration which is one of the main topics of this work.

2 TCAD Sentaurus overview

The Sentaurus TCAD (*Synopsys Inc.*) software suite is a bundle of many separated simulators and viewers which has the ability to simulate and optimize semiconductor processing technologies and devices. It solves the coupled continuity and Poisson equations under specific boundary conditions in 2 or 3 dimensions.

Following is a short description of the simulators that were used in our research:

2.1 Process Simulator - is an advanced 1D, 2D, and 3D process simulator suitable for silicon and other semiconductors. It features a modern software architecture and state-of-the-art models to address current and future process technologies. Processing steps such as etching, deposition, ion implantation, thermal annealing, and oxidation are simulated based on physical equations, which govern the respective processing steps. It can give us an idea of the limitations of real fabrication technologies.

2.2 Structure Editor and Mesh Engine - is a combined editor and mesh engine for 2D and 3D device structures. 2D and 3D device models are created geometrically, using 2D or 3D primitives, such as rectangles, polygons, cuboids, cylinders, and spheres. Complex shapes are generated by simply intersecting primitive elements. Then, doping concentration and mesh resolution are defined for each region.

The Structure Editor can be used for creating abstract models with no simulation of processing techniques. Or, it can be used as the connection between the Process and Device simulators (below), as the user is able to import the Process model to the Structure Editor, and with a few modifications, the Process model is ready for Device simulation and testing.

2.3 Device Simulator - simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations (Coupled Poisson and Continuity equations) that describe the carrier distribution and conduction mechanisms. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration.

2.4 Tecplot and Inspect Viewers - is the outputs viewers of TCAD; this programs allow the user to analyze various physical and geometrical parameters. It is with these programs that we are able to actually "see" the results and models that were simulated in the Process and the Device. It is where we see the IV and extract the efficiency, FF and etc.

2.5 Sentaurus Workbench - is the Synopsys framework tool. It is a complete environment for creating, managing, executing, and analyzing all the TCAD simulations. It allows users to navigate and automate efficiently the typical tasks associated with running TCAD simulations such as managing the information flow, including preprocessing of user input files, parameterizing projects, setting up and executing tool instances, and visualizing results with appropriate viewers. In addition Sentaurus Workbench enables users to carry out many simulations simultaneously. Figure 5 illustrates a typical flow process that can be carried out automatically by the Sentaurus Workbench.

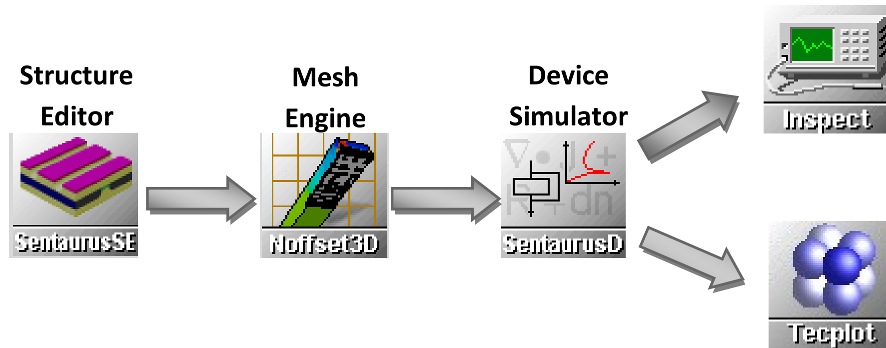


Figure 5: Example of a simulation flow process.

3 Junction modeling and optimization

A single VJ is shown in Figure 6(a), while (b) illustrates the series connection of several VJ forming a VMJ cell. Previous analyses have used approximate one-dimensional models by applying many simplifying assumptions [1]. However, a realistic VJ is an inherently two-dimensional device that must be analyzed in two dimensions. The inconsistency of using a one-dimensional approximation is discussed in detail in Section 3a below. We present here a comprehensive numerical analysis of the vertical junction under illumination with full account of the two-dimensional effects.

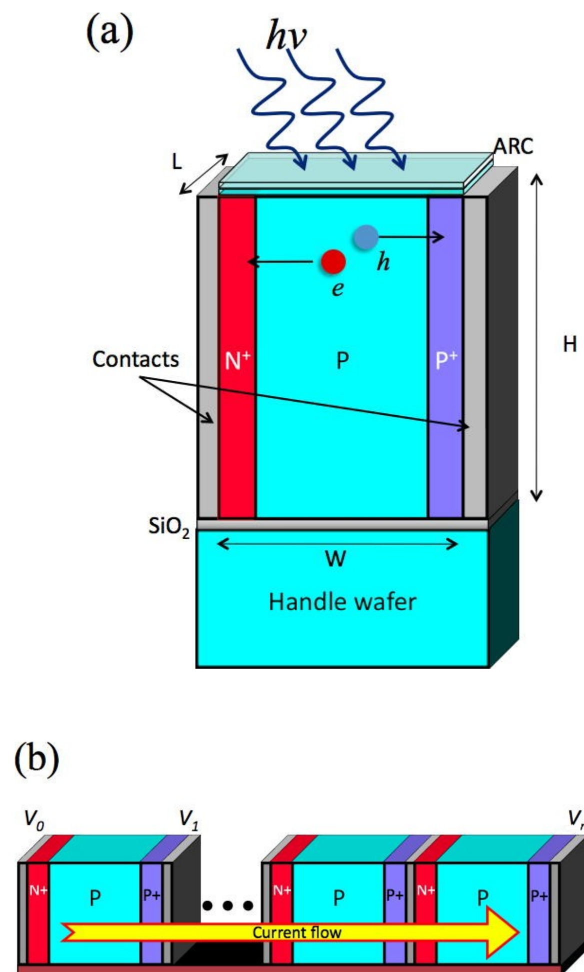


Figure 6: Schematics of a Vertical Junction (a), and a Vertical Multi Junction (VMJ) cell (b)

In the present analysis, it was assumed that the device characteristics are uniform in the third dimension, L in Figure 6(a) which permits a two-dimensional analysis.

Table 1 lists all the models used in the TCAD simulations [12].

Bulk Recombination	SRH (Doping Dependence) –*"Scharfetter model"* [12] Auger
Carrier Mobility	Doping Dependence – *"Masetti model"* [12] High Field Saturation – *"Canali model"*[12] Enormal – *"Lombardi model"* [12] Carrier Carrier Scattering – "*Conwell–Weisskopf model*" [12]
Band-Gap-Narrowing	*"Oldslootbloom model"* [12]
Surface Recombination	Surface SRH recombination

Table 1: Physical models used in the TCAD simulations.

The incident radiation was modeled using ray tracing incorporated in the Sentaurus TCAD. The solar spectrum was modeled by dividing the AM1.5G spectrum to 86 segments. The contribution of each spectral segment to the optical generation was calculated using a bundle of rays with appropriate power and wavelength. Concentrated illumination was modeled by multiplying the AM1.5G spectrum by the flux concentration ratio, *C*. It should be noted that collimated rays were used in all the simulations; hence, this is not an exact representation of concentrated illumination, as real concentrated illumination will have some angular distribution.

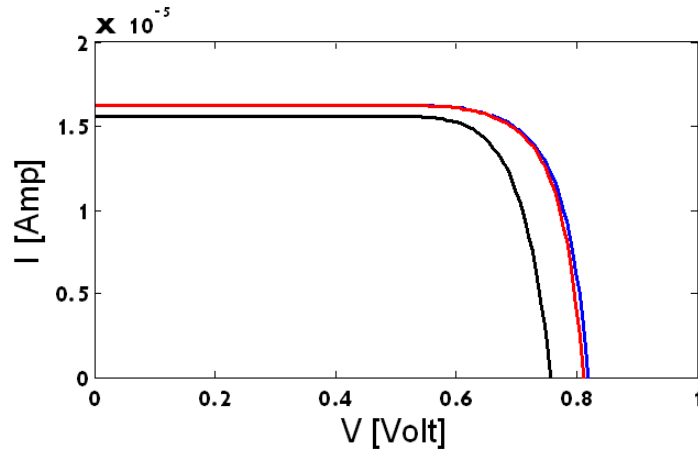
We have assumed that the VJ is implemented in a Silicon On Insulator (SOI) substrate, as shown in Figure 6(a). The Shockley-Read-Hall (SRH) bulk lifetime depends on the substrate quality and the fabrication process. A SRH lifetime of 1 ms for both electrons and holes was used, corresponding to state of the art Floating Zone (FZ) silicon substrate [13]. The back surface of the junction constitutes of 1 μm SiO_2 layer, serving also as a reflective coating (RC), on top of a silicon handle wafer, as part of the SOI. No surface treatments can be done in back surface region, leading to high back surface recombination (BSR) therefore it was assumed to be 1000 cm/s [14].

The formation of the junction is implemented by doping through the sidewalls of vertical trenches etched in the active layer. The vertical contacts between adjacent junctions are formed by filling the trenches with metal. Recombination at the side metal contacts was set to 10^6 cm/s for both electrons and holes; this high value was chosen to account for possible damage during the trench fabrication, implantation (or diffusion) through the sidewalls and the metallization interface. Lower interface recombination velocities were found to increase the efficiency by about 3%.

The metal-filled trenches constitute an inactive area and their width should be minimized relative to the width of the active junction. We assume that the trench is fabricated by etching in the active layer of the SOI wafer; hence, the main constraint on its width is set by the fabrication capabilities of narrow (high aspect ratio) trenches. An aspect ratio (trench depth, which is equals to the VJ depth, to trench width) of 20:1 was used in all the simulations. A higher aspect ratio will increase the VJ efficiency by reducing the fraction of inactive area in the junction.

Standard front surface treatments are assumed, which include texturing, passivation and optimized double anti-reflection coating (ARC). The ARC consists of 55 nm of a Si_3N_4 layer on top of a 55 nm layer of SiO_2 (Section 3.3). The front Surface Recombination (FSR) was assumed to be 100 cm/s, appropriate for these surface treatments [15].

The significance of Auger recombination was studied by running simulations at irradiance of 1000 suns with different Auger recombination coefficients. The results have shown that the losses due to this recombination mechanism are negligible: an increase of one order of magnitude in the Auger coefficients has resulted in a decrease of less than 0.06% in the VJ's conversion efficiency (Figure 7).



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The junction doping profile was modeled using a Gaussian doping profile which is defined by width and peak doping. Optimization of the junction profile was made for the left and right implant regions (Figure 6(a)). The optimized Gaussian width for both regions was determined to be 2.8 μm and the peak doping was determined to $10^{19}cm^{-3}$.

The conversion efficiency of a VJ was calculated for relevant ranges of junction design parameters (junction width and depth, doping level). The results show the optimal junction design and expected performance for a range of achievable material properties (SRH lifetime, FSR and BSR values). The simulations were repeated for different concentration levels, showing dependence of the junction performance and of the optimal junction design with concentration.

3.1 Results

3.1.1 Coupling of absorption and carrier collection

In standard horizontal cells, there is a trade-off between the collection of minority carriers due to limited diffusion length, and absorption of photons, as both effects are determined by the junction's depth. In an ideal VJ's, under the approximation of no front and back surface recombination, the carrier collection and photon absorption are

orthogonal and decoupled [1,16]. As a result, the carrier collection efficiency of the VJ is independent of the photon wavelength and the spectral response is uniform. This is due to the fact that under the above approximations, the travel distance of the free carriers is independent of the cell depth *H*. Hence, a carrier photo-generated at a certain distance from the front surface will have the same collection efficiency, even if the depth of the cell has changed. As a result, an independent optimization of the junction dimensions (width and depth) and of doping values is feasible.

As shown in [1] the short circuit current density of an ideal VJ, J_{sc}, can be written as:

$$J_{sc}(\lambda, z, W) = q\eta_a(\lambda, z)\eta_{coll}(W)N(\lambda) \tag{1}$$

Where q is the electron charge, $\eta_a(\lambda,z)$ is the absorption efficiency for wavelength λ at depth z, $\eta_{coll}(W)$ is the collection efficiency for cell width W, and $N(\lambda)$ is the intensity for wavelength λ. The total short-circuit current is obtained by integrating Eq. (1) over the depth z and wavelength λ:

$$I_{sc}(H, W) = \int_0^\infty \int_0^H q\eta_a(\lambda, z)\eta_{coll}(W)N(\lambda)dzd\lambda = \eta_{coll}(W)f(H) \tag{2}$$

Where $f(H)$ is independent of the cell width W. Dividing the short circuit current of two VJ's with equal width but different depths, we obtain for the ideal case no dependence on W:

$$\frac{I_{sc}(H_1, W)}{I_{sc}(H_2, W)} = \frac{f(H_1)}{f(H_2)} \tag{3}$$

Figure 8 shows the ratio defined in Eq. (3) as calculated from the full two-dimensional simulation for junctions of the same width and of depths of 60 and 200 μm, for the ideal case of BSR=FSR=0, and for the realistic case of FSR=500 cm/s, BSR=1000 cm/s. When there is no surface recombination, the ratio is nearly independent of the junction width as predicted by Eq. (3). On the other hand, the ratio increases significantly with the junction width when the surface recombination is non-zero. This indicates that the photon absorption and carrier collection are no longer decoupled as in the ideal case. The simplified models that

assume one-dimensional behavior [1] are therefore inadequate, and a two-dimensional simulation is required.

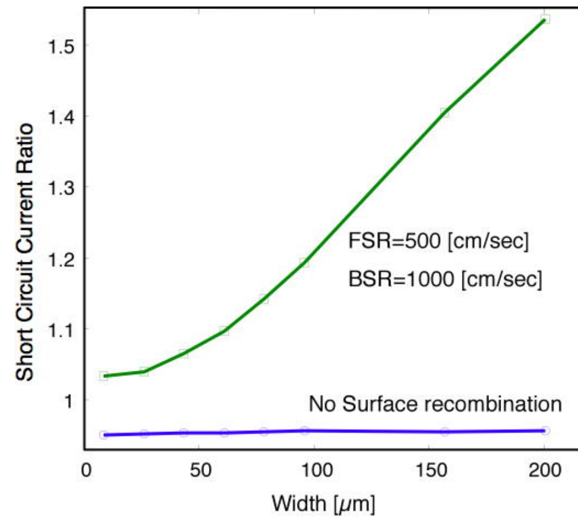


Figure 8: Ratio of short circuit currents of VJ's having 200μm and 60μm depths, as a function of VJ width, with and without surface recombination.

3.1.2 Effect of surface recombination

Figure 9 shows the VJ efficiency for different widths and FSR velocities under irradiation of 1 and 1000 suns. The value of the BSR velocity is fixed for both cases. The increase of FSR velocity decreases the VJ efficiency, as expected. For each value of FSR, an optimum junction width can be clearly observed. For low FSR, the optimum is quite broad, allowing flexibility in the selection of width; but at higher FSR the optimum is steeper. In addition, higher FSR also decreases the optimal VJ width. The efficiency values and the decrease in efficiency with increasing FSR, as seen in Figure 9(a), are similar to the values and the trend shown for the "practical parameters" case in [11]. The results are not identical due to differences between the two simulations: [11] separates the effects of surface recombination of holes and electrons, and assumes that the surface recombination velocity of both surfaces is equal.

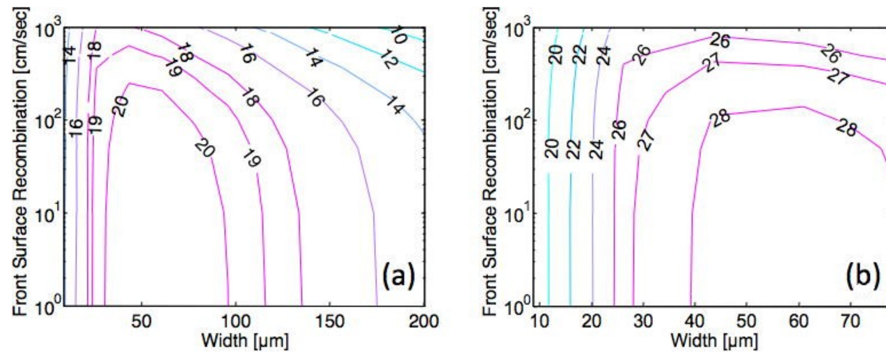


Figure 9: Efficiency vs. width and front surface recombination velocity for BSR=1000 cm/s under 1sun (a) and 1000 sun (b)

Figure 10 shows the variation of the VJ efficiency with the junction dimensions, for different combinations of FSR and BSR velocities. The optimal values for both of the junction dimensions, width and depth, are affected by the recombination velocities. When the surface recombination is very low, the optimal junction width is higher than 200 µm as seen in Figure 10(a), and may reach the magnitude reported in [11]. However, high surface recombination lowers the optimal width: for example, increasing FSR to 100 cm/s and 500 cm/s while keeping BSR low, the optimal junction width is around 150 µm and 70 µm, respectively, as seen in Figure 10(c) and (e).

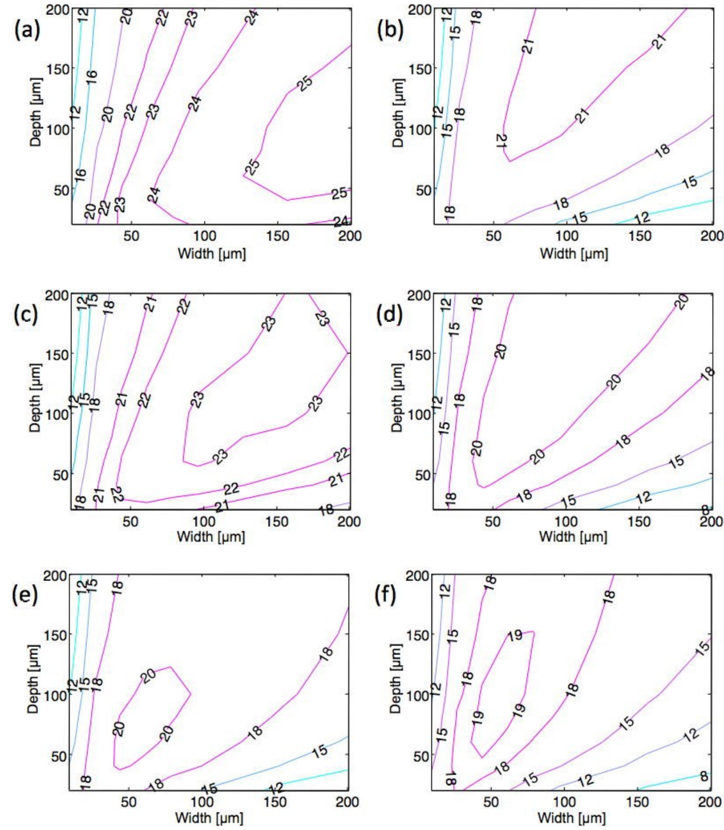


Figure 10: VJ efficiency vs. width and depth: 1sun, FSR= 10 cm/s, BSR=0 cm/s (a), 1sun, FSR=10 cm/s, BSR=1000 cm/s (b) ,1sun, FSR=100 cm/s, BSR=0 cm/s (c), 1sun, FSR=100 cm/s, BSR=1000 cm/s (d), 1sun, FSR=500 cm/s, BSR=0 cm/s (e), 1sun, FSR=500 cm/s, BSR=1000 cm/s (f)

The significant effect of surface recombination on the efficiency of PV cells is well known. In horizontal junctions, minority carriers that are generated close to the front surface pass a short distance before they cross the junction away from the surface, as seen in Figure 11. Therefore, higher cell width does not increase the effect of the front surface recombination. In contrast, in the VJ, minority carriers created close to the surface will have an average traveling distance of $W/2$ before reaching the junction. Since a large fraction of the charge carriers is generated close to the front surface, the FSR will have a large effect on the VJ efficiency and the selection of optimal width.

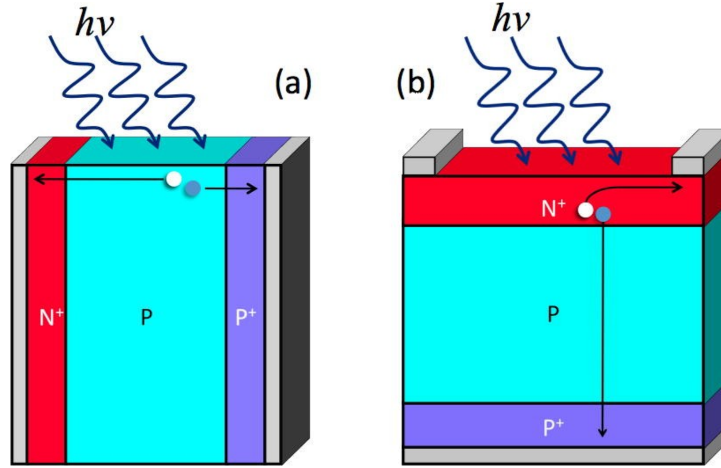


Figure 11: Surface recombination effect: typical carrier paths in a vertical junction (a) and a horizontal junction (b)

High BSR moves the junction design optimum toward larger depth, creating a larger distance between the back surface and most of the charge carriers. For example, the optimal depth is above 200 µm for BSR=1000 cm/s compared to only around 100 µm for BSR=0, as seen in Figure 10(c) and (d), respectively.

3.1.3 Effect of SRH lifetime

The SRH lifetime value was set in the simulation according to:

$$\tau = \frac{\tau_{max}}{A} \tag{4}$$

A is a constant defined by the doping levels [17], and τ_{max} is the SRH value of the intrinsic FZ silicon substrate. When considering the VJ's sensitivity to SRH lifetime, the parameter τ_{max} was varied between 1 µs and 1 ms, and A was modified according to the doping level in each region in the VJ.

Figure 12(a) and (c) shows the variation of the VJ efficiency with SRH lifetime and the junction width for 1 and 1000 suns, respectively. A correlation can be seen between the SRH lifetime and the optimal junction width: for the shortest lifetime the optimal width is 20—30 µm, while for longer lifetime the optimal width increases to 50—60µm. This dependence is expected since the junction width determines the path length for carrier collection.

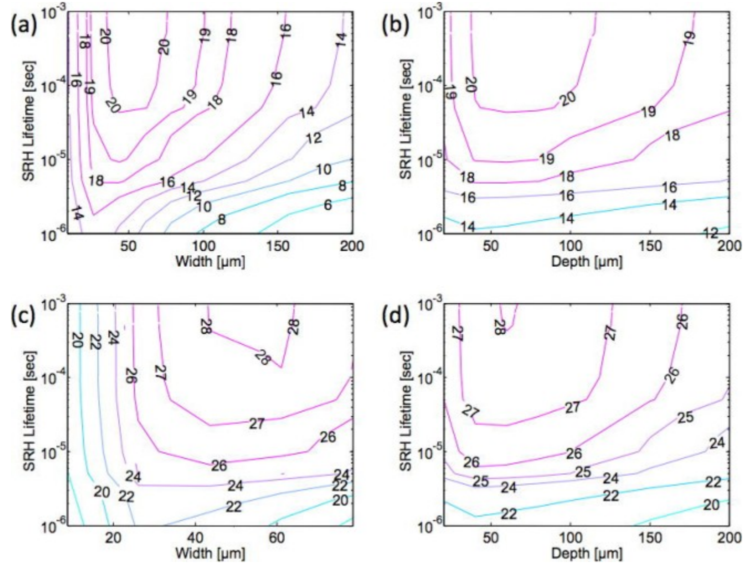


Figure 12: Efficiency vs. width and SRH lifetime, 1sun (a); efficiency vs. depth and SRH lifetime, 1sun (b), efficiency vs. width and SRH lifetime, 1000 suns (c); efficiency vs. depth and SRH lifetime, 1000 suns (d).

While carrier lifetime prevents the optimal junction width from growing, another effect prevents it from shrinking. When the junction width is very small, the built-in voltage of the cell decreases significantly. This is the case of a quasi "short" diode, where the quasi-neutral region is smaller than the carrier diffusion length and more recombination take place at the contacts. As a result, the separation between the quasi-Fermi levels of electrons and holes decreases and this lowers the cell V_{oc} and the overall efficiency.

Figure 12(b) and (d) shows the variation of the VJ efficiency with SRH lifetime and the junction depth for 1 and 1000 suns, respectively. The optimal junction depth seems to be insensitive to the SRH lifetime. This is consistent with the understanding that the lifetime mostly affects the carrier collection and therefore has a strong effect on the junction width, but no direct interaction with the junction depth.

3.1.4 Effect of bulk doping

As the SRH lifetime, mobility and bulk conductivity are all doping dependent, the central region doping affects the VJ performance significantly. Increasing the bulk doping decreases the bulk resistivity on the one hand, but decreases the minority carrier lifetime and mobility on the other; therefore, there is a tradeoff between the bulk resistivity and the carrier collection as shown in Figure 13. Low mobility and

low carrier lifetime caused by high bulk doping create a preference for the use of narrow VJs. This can be seen in Figure 13(a) and (b), for 1 sun and 1000 suns, respectively. The VJ optimal width decreases when the bulk doping is above a certain value, as shown by the dashed lines. On the other hand, there are also consequences to lowering the doping too much: the mobility, SRH lifetime increase but the cell resistivity also increases, leading to an optimal dopant concentration as seen in Figure 13(a).

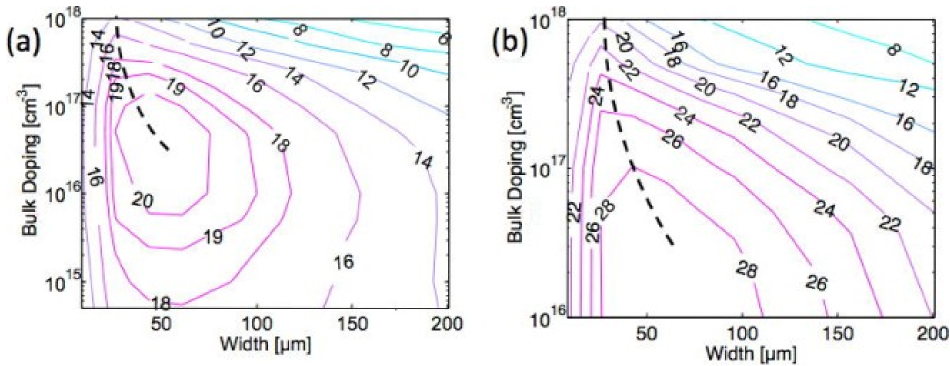


Figure 13: Efficiency vs. junction width and bulk doping, 1sun (a), 1000 suns (b); dashed lines show the location of the optimal width for each doping level

3.1.5 Effect of concentration

Figure 14 shows the efficiency of VJs with several combinations of junction depth and surface recombination velocities, as a function of the concentration level. The efficiency continues to increase for concentration levels well over a 1000. The saturation of the efficiency at high concentrations can be attributed to the series resistance. This effect is more dominant in shallower junctions, Figure 14(a) and (b), as their cross section area is smaller, leading to higher series resistance. The low efficiency of the deeper junctions, Figure 14(c) and (d), is purely a result of the loss of active area by the contact trenches.

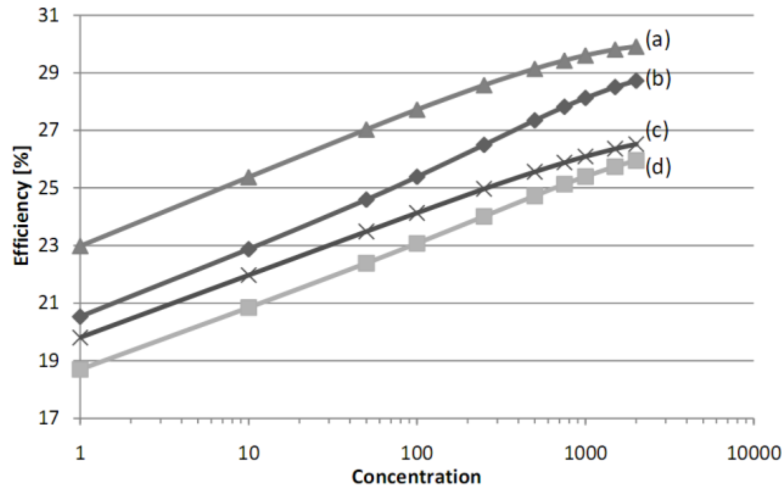


Figure 14: Efficiency as a function of solar flux concentration for a VJ of width 43.6 µm and depth 60 µm, FSR=0, BSR=0 cm/s (a), depth of 60 µm, FSR=10, BSR=1000 cm/s (b), depth of 200 µm, FSR=10, BSR=0 cm/s (c), depth of 200 µm, FSR=10 µm, BSR=1000 cm/s (d).

Before discussing further the VJ series resistance, let us examine the various series resistance components of a horizontal junction (Figure 15): (a) current flow through the emitter and bulk of the solar cell; (b) the contact resistance between the metal contact and the Silicon, and finally (c) the resistance of the top and rear metal contacts. The resistance of the Si bulk is usually insignificant and because of that is negligible.

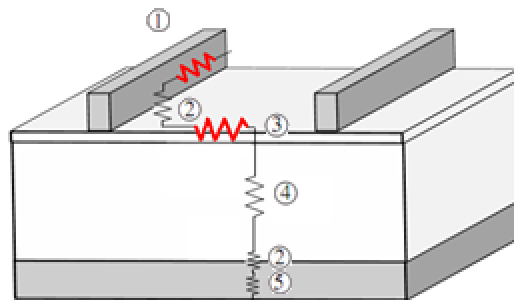


Figure 15: Schematic representation of the components of the series resistance in the horizontal junction: 1. metal resistance; 2. metal- semiconductor contact resistance; 3. emitter - P+ region resistance; 4. bulk resistance; 5. back surface field - N+ region resistance. The red resistors are the dominant resistance components.

The metallic top contacts are necessary to collect the current generated by a solar cell. "busbars" are connected directly to the external leads, while "fingers" are finer

areas of metallization which collect current for delivery to the busbars. The key design trade-off in top contact design is the balance between the increased resistive losses associated with a widely spaced grid and the increased reflection caused by a high fraction of metal coverage of the top surface.

The distance that the current flows in the emitter is not constant. Current can be collected from the base close to the finger and therefore has only a short distance to flow to the finger or, alternatively, if the current enters the emitter between the fingers, then the length of the resistive path seen by such a carrier is half the grid spacing (Figure 16)

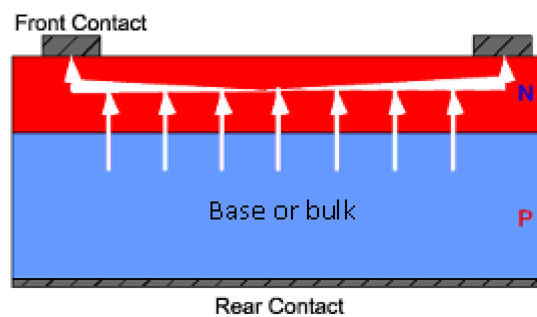


Figure 16: Current flow from the base to the fingers

The VJ has inherently lower series resistance and lower current density, and therefore is able to maintain high efficiency at much higher concentration, compared to a horizontal junction cell. However, the simulation results reveal that this is not the only effect responsible for the high performance of the VJ under high concentration. In the VJ, the current flows nearly entirely in the horizontal direction and the series resistance will be the sum of the components shown schematically in Figure 17. Compared to standard horizontal junction, the series resistance does not include an emitter sheet resistance, or resistance of a metal grid having a very small cross section area. The current flows perpendicular to the highly doped layers and the metal contacts that have a large cross section area, therefore their resistance is negligible. As the contact area is much larger relative to horizontal cells, the metal-semiconductor contact resistance will also be small. The light doping and the relatively large width of the bulk region make the bulk resistivity the dominant component in the series resistance. The conductivity at each point in the cell can be calculated according to:

$$\sigma(x,y) = q\left[p(x,y)\mu_p + n(x,y)\mu_n\right] \quad (5)$$

q is the electron charge, *p* and *n* are the holes and electron concentrations, respectively, and μ_n, μ_p are the electron and hole mobilities.

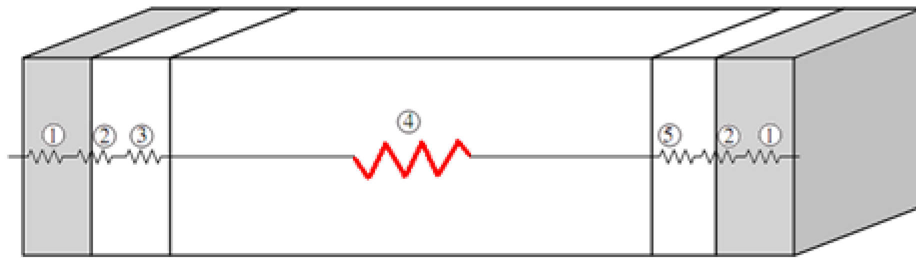
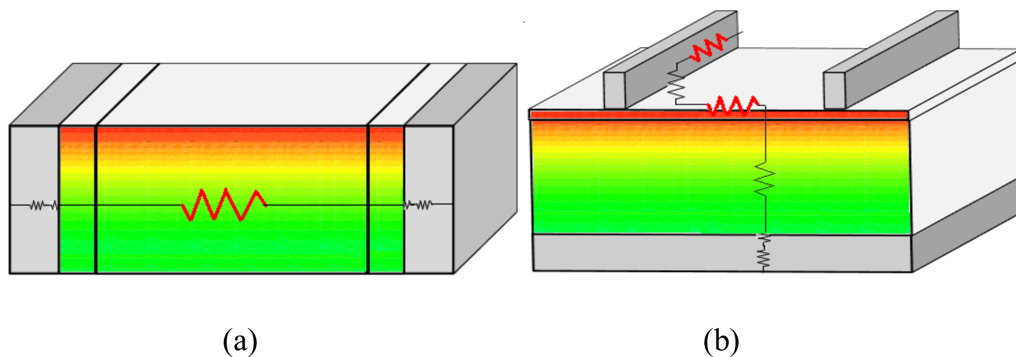


Figure 17: Schematic representation of the components of the series resistance in the VJ: 1. metal resistance; 2. metal- semiconductor contact resistance; 3. P+ region resistance; 4. bulk resistance; 5. N+ region resistance

Since the bulk is lightly doped, high concentration may cause an increase by orders of magnitude in the charge carrier concentration, resulting in a large photoconductivity effect that significantly reduces the series resistance of the VJ. The most significant reduction occurs at the top of the junction. In conventional cells, this effect will be negligible because the emitter is always heavily doped, making the increase in charge carriers concentration negligible (Figure 18).



(a) (b)

Figure 18: Schematic representation of the photoconductivity effect caused by the high concentration in the VJ (a); horizontal junction (b)

The VJ resistivity was calculated from the simulation results at selected location in the junction: at the middle of the VJ at depths of 5, 10, 20, 30, 40 and 50 µm. Figure 19 shows the dramatic reduction in local resistivity at these locations under increasing concentration levels. The photoconductivity effect is the strongest at location near the top of the junction, where most of the carriers are generated. This

decrease in bulk resistivity in the junction helps to delay the impact of the series resistance as the concentration increases, leading to outstanding performance at concentration levels well above 1000.

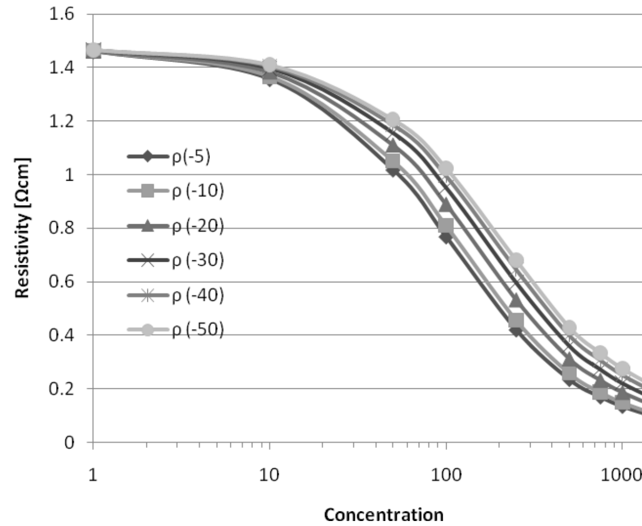


Figure 19: Bulk resistivity at selected locations as a function of flux concentration

Figure 20 shows the VJ efficiency as a function of flux concentration and bulk doping. The dashed line indicates the optimal bulk doping for each concentration. It can be easily seen that the optimal bulk doping decreases slightly with the concentration. Decrease in the bulk doping increases the bulk resistivity and the carrier mobility; this indicates that even under high concentration, losses attributed to the series resistance are still insignificant comparing to the recombination losses.

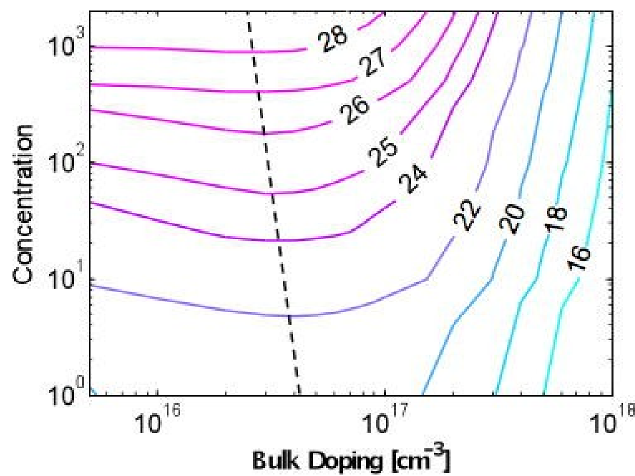


Figure 20: Efficiency vs. bulk doping and concentration

Figure 21 shows a comparison of the VJ efficiency with other vertical junction designs [2, 6] and other concentrator Si cells [18]. The VJ presented here (a) is strongly affected by surface recombination due to the specific fabrication process, and therefore its conversion efficiency is lower under low and moderate concentration than cells with front surface diffusions (c) and standard horizontal cells (b). However, under high concentration, the diffusion layers in the latter cells lead to increased series resistance losses which decrease the conversion efficiency dramatically. The vertical junction cell tested by Sater (d) exhibit very low series resistance losses as its efficiency peaks at nearly 1500 suns. However, the efficiency value of around 20% at high concentration is far below the potential of well optimized VMJ cells as shown here. A simulation of a junction 250 µm wide and 500 µm deep with surface recombination velocities between 200-500 cm/s and SRH lifetimes τ_{max} = 0.25 ms has confirmed efficiencies similar to those reported in [2] and [11], and the conclusion is that the junction dimensions are responsible for the low efficiency realized in the past.

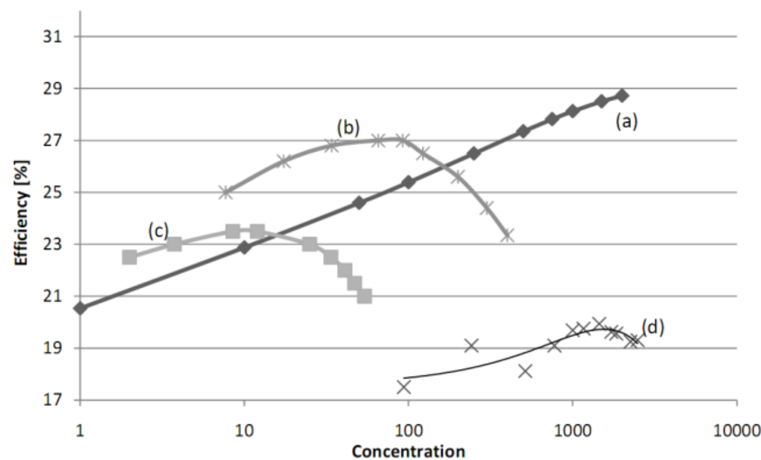


Figure 21: Conversion efficiency as a function of solar flux concentration: VJ of width 43.6 µm and depth 60 µm, BSR=1000 cm/s and FSR= 10 cm/s (a); Slade at al. [18] (b); Sliver cell [10] (c); Sater at al [2] (d)

3.2 Calculating the series resistance using simple electric assumptions

The resistivity at selected locations inside the VJ has been presented at Figure 19 as a function of concentration. We believe that the total conductivity (or resistance) of the junction behaves in the same manner.

Calculating the series resistance of the VJ is not straight forward, and even simplifying assumptions are not beneficial in this case. The main flow of the charges is in the bulk and because of the nature of the VJ, the carriers' path is elliptic. The resistance formula ($R = \frac{\rho L}{A}$) is based on perpendicular transport between two electrodes. In a horizontal junction, this assumption can be applied to the busbars, fingers and to the emitter region. The bulk is not a critical element in the overall resistance and thus can be neglected. However, in the VJ, because of the elliptic movement inside the bulk region, this perpendicular movement assumption is not valid.

Traditional methods to extract the series resistance from the IV curve are not useful in the case of the VJ. They are based on assumptions that are not applicable in the VJ such as: series resistance isn't affected by illumination intensity; series resistance is constant for every applied voltage and more.

Because of the inability to make any simplified assumptions or use known techniques, we have decided to calculate the series resistance using a model which is based on simple electric model in order to get an approximate results.

The series resistance can be approximated as the resistance that each charge carrier experiences for all possible paths from one electrode to the other. We have calculated only the bulk resistance, which is the main resistance component.

In order to calculate the series resistance in the bulk region, we used the bulk conductivity map $\sigma(x, y)$ calculated by Sentaurus TCAD.

In our model, the bulk has two electrodes covering two opposite edges at x=0 and x=L. The boundary conditions forced by the electrodes are $V(x=0)=V_1$ on one side of the bulk and $V(x=L)=V_2$ on the other.

Since $\vec{J} = \sigma\vec{E} = -\sigma\vec{\nabla} V$, and since there can be no current in the Y direction along the top and bottom boundaries of the problem, two other boundary conditions are

$$\left.\frac{\partial V}{\partial y}\right|_{y=0} = \left.\frac{\partial V}{\partial y}\right|_{y=D} = 0 \qquad (6)$$

Assuming that the electrodes are perfect conductors turns the above to:

$$\left.\frac{\partial V}{\partial y}\right|_{p} = 0 \tag{7}$$

where p is the boundary of the problem. Figure 22 shows the problem and its boundary conditions.

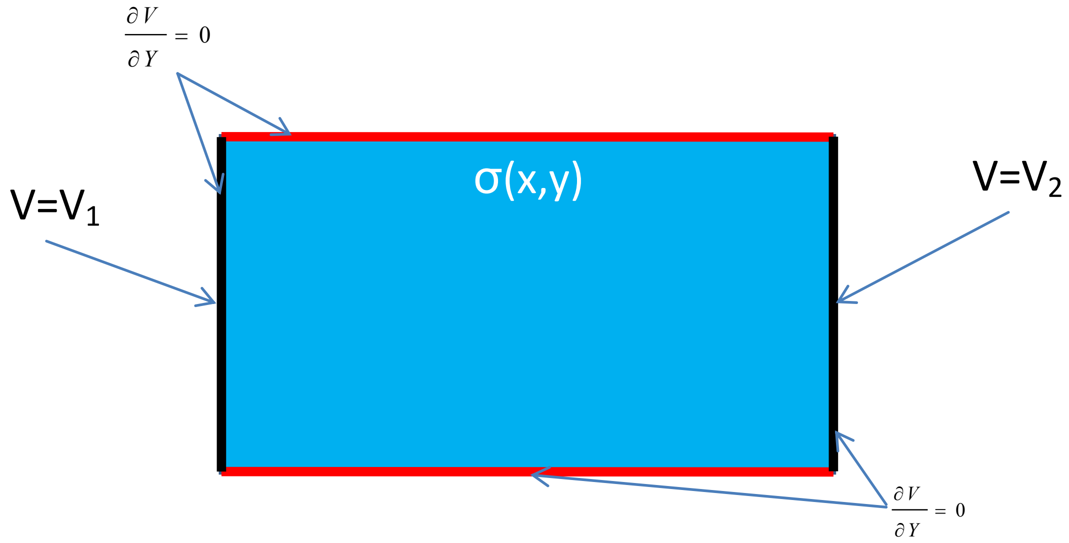


Figure 22: The bulk region with its boundary conditions.

Under the above conditions, the series resistance can be calculated to be:

$$R_s = \frac{V_2 - V_1}{I} \tag{8}$$

where I is the total current flowing through the bulk. Assuming that the electrodes are perfect conductors, the potential difference between every point in the left electrode and every point in the right electrode will be V_2-V_1. Hence, for every line l that starts at $x=0$ and ends at $x=L$

$$-\int_l \vec{E}\,d\vec{l} = V_2 - V_1 \tag{9}$$

This is specifically true for lines parallel to the x axis:

$$-\int_0^L \vec{E}\,d\vec{x} = -\int_0^L E_x\,dx = V_2 - V_1 \tag{10}$$

Since V_2-V_1 is independent of y, the integral must be as well. For this reason E_x=$E_x(x)$.

As stated above, I is the total current flowing through the bulk:

$$I = \int \vec{J}\Big|_{x=0} d\vec{A} \tag{11}$$

Assuming steady state and DC operation, the current must be constant for every cross-section along the x axis.

$$\int \vec{J} d\vec{A} = const = I \tag{12}$$

Taking $d\vec{A}$ to be $dydz \cdot \hat{x}$ and assuming the problem to be two dimensional, we obtain

$$w \int_0^D \vec{J} dy \cdot \hat{x} = w \int_0^D J_x dy = I \tag{13}$$

where w is the magnitude of the cell in the third dimension. Substituting $J=\sigma E$ and rearranging:

$$\int_0^D \sigma E_x dy = \frac{I}{w} \tag{14}$$

From Eq. (5) we know that E_x does not depend on y which allows us to isolate the electric field in the x direction:

$$E_x = \frac{I}{w \int_0^D \sigma dy} \tag{15}$$

Substituting Eq. (10) into Eq. (5) we receive:

$$V_2 - V_1 = \int_0^L \frac{I}{w \int_0^D \sigma dy} dx \tag{16}$$

Since we assumed that the total current is constant:

$$R_s = \frac{V_2 - V_1}{I} = \int_0^L \frac{1}{w \int_0^D \sigma dy} dx \tag{17}$$

From Eq. (17), we derived the bulk resistance which is shown in Figure 23. The conductivity map was calculated by Sentaurus TCAD for different concentration levels.

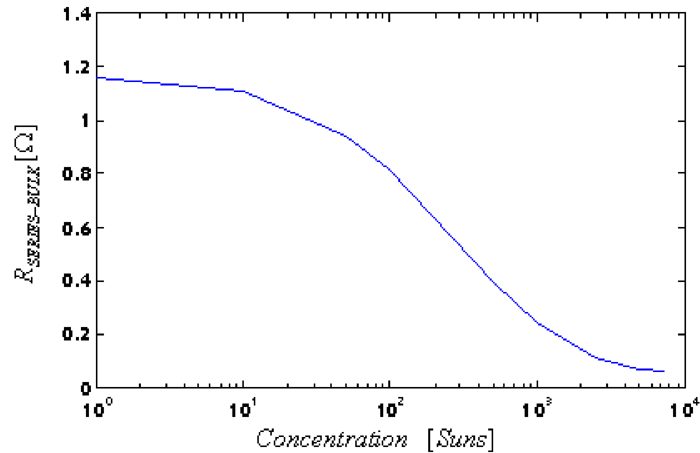


Figure 23: Behavior of the VJ bulk resistance as a function of concentration

3.3 Light trapping

Optical losses consist of light which could have generated an electron-hole pair, but does not, because the light is either reflected from the front surface, or because it is not absorbed in the solar cell.

There are a number of ways to reduce the optical losses:

- Anti-reflection coating can be used on the top surface of the junction.
- Reflective coating can be used on the back surface of the junction.
- Surface texturing on the top surface of the junction.
- Contact coverage of the junction can be minimized (Depends on the aspect ratio of the trench). Angular trenches and partially filed trenches are also a possibility.

3.3.1 Anti reflecting coating

Anti-reflection coatings on solar cells are similar to those used on other optical device such as camera lenses. They consist of a thin layer of dielectric material, with a specially chosen thickness so that interference effects in the coating cause the wave reflected from the anti-reflection coating top surface to be out of phase with the wave

reflected from the semiconductor surfaces, as we can see in Figure 24. These out-of-phase reflected waves destructively interfere with one another, resulting in zero net reflected energy.

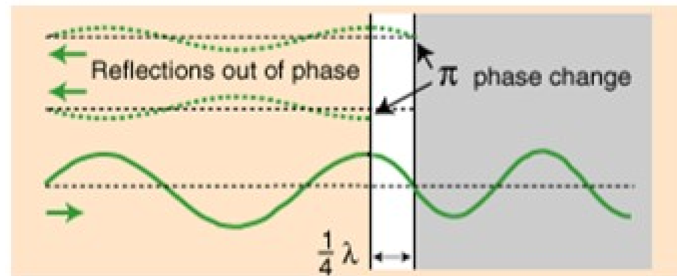


Figure 24: Anti-reflective coating explanation

Reflection Phase Change - reflected light will experience a 180 degree phase change when it reflects from a medium of higher index of refraction and no phase change when it reflects from a medium of smaller index. This phase change is important in the design of anti-reflection coatings, and thin film mirrors. In our case we have 3 kinds of mediums first the air medium (n_1) second the thin film medium (n_2) and third, the Silicon medium (n_3) so $n_1<n_2<n_3$ and we have two phase changes caused by the mediums. The thickness of the thin film causes a destructive reaction of the reflected light.

The reflection for a given index of refraction can be reduced for a specific wavelength because the index of refraction depends on wavelength.

The anti reflective is also used for passivation of the front surface.

3.3.2 Reflective coating.

The depth of the VJ is a problematic issue due to:

- The required depth of the cell is determined according to the absorption coefficient of the silicon substrate.
- Deeper junction lead to deeper trenches which leads to higher metal coverage and even higher aspect ratio due to fabrication limitations.
- Deeper junction reduces the VJ voltage (Appendix 7.1).

The main objective of the reflective coating is to reduce the depth of the cell while maintaining the same absorption depth. This can be done in the same way as

anti reflective coating but this time we need to create a constructive reaction for the light.

A SOI substrate is used to fabricate our VJ so we use the buried SiO_2 as a reflective surface. That means that we have 3 kinds of mediums: first the Si active surface medium (n_3) second the thin film medium (n_4) and third the Silicon handler (n_5) so $n_3>n_4<n_5$ and we have one phase change caused by the mediums and the thickness of the thin film causes a constructive reaction of the reflected light.

3.3.3 Absorption depth

The dependence of the absorption coefficient on wavelength causes different wavelengths to penetrate to different distances into the semiconductor before most of the light is absorbed. The absorption depth is given by the inverse of the absorption coefficient, or α^{-1}. It indicates the distance where the intensity of the light drops to 36% of its original intensity, or alternately has dropped by a factor of 1/*e*.

Energetic photons has large absorption coefficient. Therefore, they are being absorbed within a few microns from the surface in the case of Silicon. Less energetic photons may need a few hundred microns to be completely absorbed. According to Figure 25, we can see that without using any light trapping technique, the cell depth needs to be somewhere around 500-1000um in order to absorb most of the light.

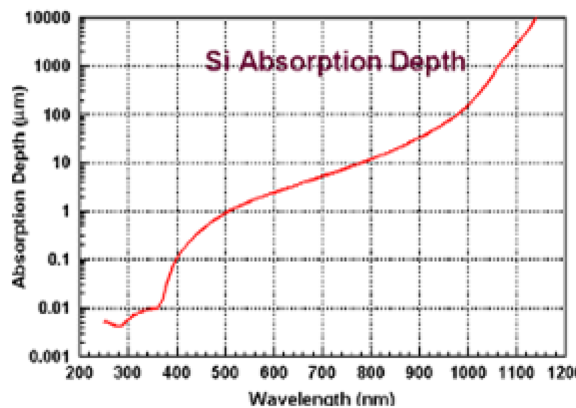


Figure 25: Absorption depth for silicon

3.3.4 Optimization of anti reflective coating and reflective coating

For the calculation of the thickness of the ARC, the minimization of the reflectivity is done for the $0.6\mu m$ wavelength. This is because of the high sunlight intensities in the region between 0.45-$0.75\mu m$.

For the calculation of the thickness of the RC, the chosen wavelength is $0.9\mu m$. The reasons for this choice are: (a) the sunlight intensity in the region between 0.84-0.93um is relatively high; (b) it is more probable that this wavelength will be absorbed in a shallow junction depth which is the case in our SOI substrate.

3.3.5 Reflection.

The reflectivity of light from a surface depends on the refraction index of the two media. We can calculate the reflectivity using:

$$R = \left(\frac{n_2 - n_1}{n_2 + n_1} \right)^2 \tag{18}$$

The refraction index is wavelength dependent. We can see in Figure 26 the relation between the refraction index and the wavelength for a silicon surface.

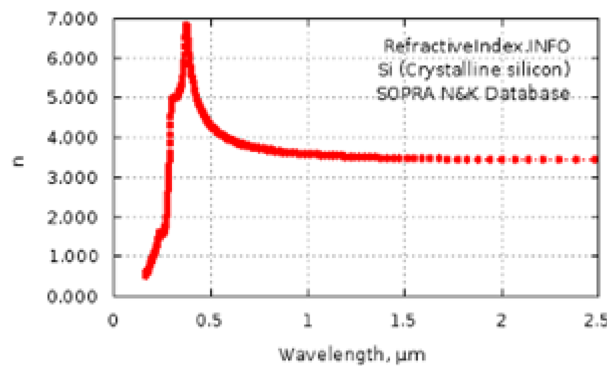


Figure 26: Relation between the refraction index and the wavelength for a silicon surface

In order to determine the reflectivity of the surface without coatings we used the Synopsys TCAD Sentaurus simulation tool and we receive the results shown in Figure 27.

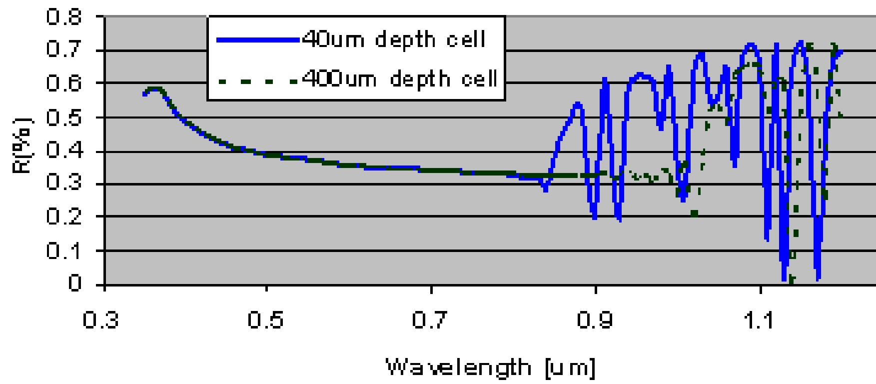


Figure 27: Reflectivity of a cell without coatings

Figure 27 show irregularities in the reflectivity at high wavelengths. This is due to the reflectivity from the second interface of air and Silicon at the bottom of the cell. In the deeper cell ($400\mu m$ cell) this behavior begins at a higher wavelength than in the shallow cell ($40\mu m$ cell). This is because of the absorption depth of the higher wavelength.

Figure 28 shows the reflectivity of the surface with the optimized ARC and with combined optimized ARC and RC.

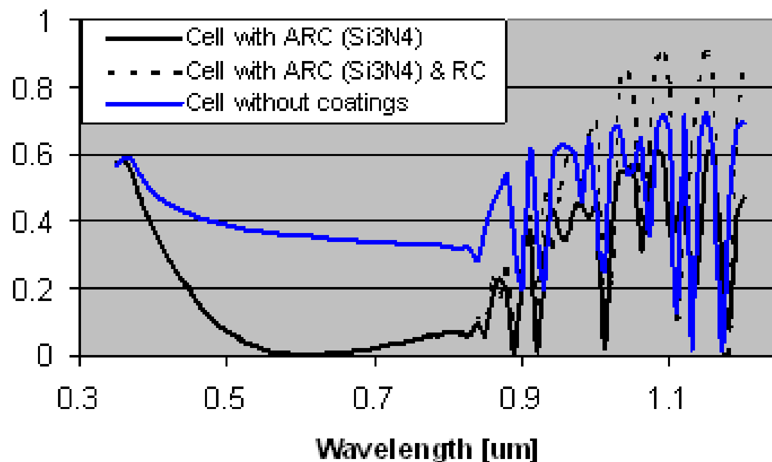


Figure 28: Reflectivity for 40um depth cell with different coatings. Blue line –no coatings, Black line – ARC, Dashed line – ARC and RC

The reflectance of the VJ with the ARC is much lower than the reflectance of the VJ without coatings (R=15%, R=40% respectively). The ARC consists of 55 nm of a $S_{i_3}N_4$ layer on top of a 55 nm layer of S_iO_2 .

The transmission of light from the bottom of the junction is lower with the RC than without the coating (T=6%, T=10% respectively). The reflectivity of the junction with RC in the lower wavelengths is the same as for a junction without RC. But for the higher wavelengths, the reflectivity is higher than for a junction without RC. This is due to the fact that not all the light that reflected from the bottom of the junction is absorbed in the cell. So the total reflectivity of a junction with RC is higher than that of a junction without RC (R=18%, R=15% respectively) but overall, more light is absorbed in the junction. Because of that the efficiency of a junction with RC is higher.

The thickness of the RC is 1 μm for the wavelength of 0.9 μm. The choice of SiO_2 as a RC is not optimal but can not be replaced because of the use of the SOI substrate. In the case of horizontal junction, the RC is usually optimized for other wavelength because the depth of the junction is much larger and the effect that has been shown in Figure 24 for a junction with depth of 40μm doesn't exist.

3.3.6 Surface Texturing

Surface texturing, either in combination with an anti-reflection coating or by itself is used to minimize reflection. Any "roughening" of the surface reduces reflection by increasing the chances of reflected light bouncing back into the surface, rather than out to the surrounding air as shown in Figure 29.

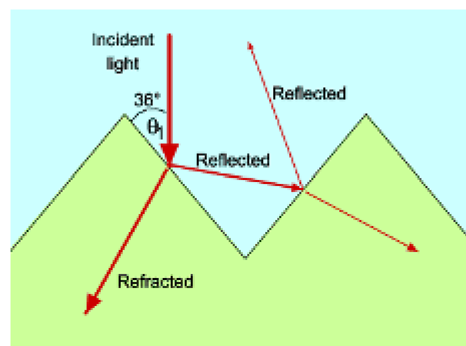


Figure 29: Reflection of light for a textured surface

Another advantage is "light trapping" in which the optical path length is several times the actual device thickness, where the optical path length of a device refers to the distance that an unabsorbed photon may travel within the device before it escapes out of the device. This is usually defined in terms of device thickness.

For example, a solar cell with no light trapping features may have an optical path length of one device thickness, while a solar cell with good light trapping may have an optical path length larger then the length of the device, indicating that light bounces back and forth within the junction.

Light trapping is usually achieved by changing the angle at which light travels in the solar cell by having it incident on an angled surface. A textured surface will not only reduce reflection as previously described, but will also couple light obliquely into the Si, thus giving a longer optical path length than the physical device thickness.

TCAD Sentaurus has showed us that the optical path is more then 2 times the depth of the VJ. So for a device with 40µm depth the optical path is a about 100µm. The fact that the optical path is longer than the depth of the VJ is very important because the depth of the VJ is limited by fabrication methods and also because of the reduction of the voltage as a function of the depth.

The VJ length is considerably small so the optical path is also affected by the metal contacts. This attribute does not exist in a horizontal junction because the size of the junction is much larger and there are no metals inside.

Table 2 shows the improvement in the VJ when applying the various surface treatments:

Texturing method	Efficiency [%]
None	X
ARC	X+5.8
ARC, RC	X+6.2
RC, Pyramides	X+7.6
ARC, RC, Pyramides	X+8.7

Table 2: Efficiency as a function of texturing method

3.3.7 Metal coverage effects

In the VJ, the contact coverage depends on the trench width. Narrow trenches are required to increase the junction active area, but this is limited by fabrication technologies.

In this following set of simulations, the VJ's efficiency was calculated for various contact sizes. We define the Metal Coverage Ratio (MCR) to be the ratio between the depth filled by the metal and the trench's depth. An approximation of the series resistance was also calculated by:

$$R_s \approx -\frac{dV}{dI}\bigg|_{V=V_{oc}} \quad (19)$$

An important assumption used was that the exposed area in the trenches can be passivated. Hence, the surface recombination velocity in this area was taken to be 100cm/sec. In order to witness the series resistance losses caused by the partial filling of the trenches, the concentration was taken to be 1000 suns (collimated rays).

An important effect that we expect to see when lowering the MCR is the reduced losses caused by surface recombination. Since the surface recombination is lower in the exposed (passivated) areas than it is in the metal-semiconductor interface, low MCR will reduce the surface recombination losses. A second important effect will be the increase in the series resistance. In low MCR values two important series resistance elements are increased. First, the conductor's resistance increases because of the decreased cross section area. A second component will be the introduction of sheet resistance in the N^+ and P^+ layers.

A third effect caused by the lowering of the MCR will be the increase in the effective active layer area. Since concentrated radiation is non-collimated, high absorbance is expected in the exposed high aspect ratio trenches. Such effect is not taken into account in this simulation.

Figures 30(a) and (b) shows the efficiency and series resistance for different values of MCR respectively. As expected a tradeoff can be noticed between the

increase in efficiency due to the lower surface recombination and the increase in series resistance.

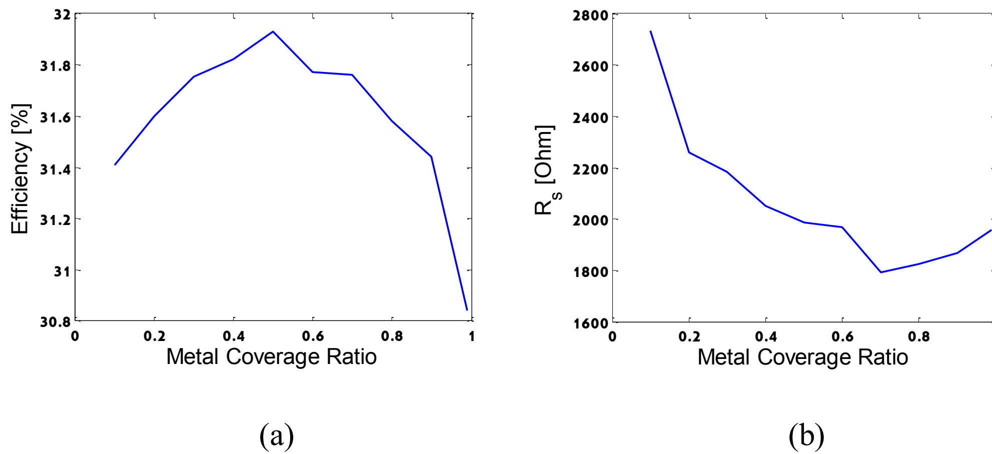


Figure 30: a. efficiency as a function of MCR, b. R_s as a function of MCR

3.3.8 Angular trenches

The recombination at the top surface has the greatest influence; but, because of our small junction dimensions, minimizing the contacts recombination can also contribute to the overall efficiency. It can be done by using the MCR approach (section 3.3.7) in combination with fabricating angular trench as shown in Figure 31.

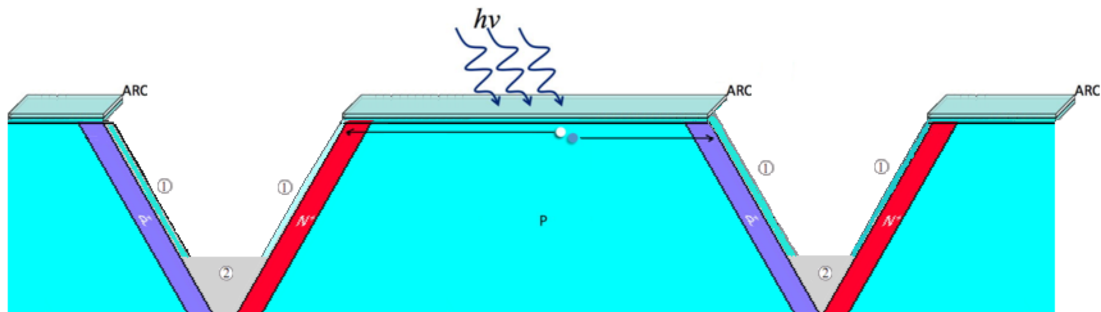


Figure 31: Partially metal coverage and angular trenches scheme: 1. passivation layer on the sidewalls of the trench; 2. localized contacts

The advantages of this design are: (a) passivation layer on the sidewalls of the trench reduces surface recombination; (b) localized contacts reduce recombination; (c) light can enter the junction from the trench sidewalls; (d) improved light trapping compared to the original junction design.

The disadvantages of this design are: (a) fabrication of partial filled contact and passivation of the exposed parts of the trench sidewalls is not trivial. Also, the coating at the top of the junction and the coating on the trench sidewalls need to be with different thickness because of the angle of the incoming light which complicates the fabrication even further; (b) series resistance becomes higher than that of the original VJ design as discussed in section 3.3.7.

This junction efficiency is improved by 1% absolutely in comparison to our best junction design when no surface recombination is applied, due to the better light trapping. When applying surface recombination, the efficiency improves by more then 1% due to the combined improvement of light trapping and less surface recombination.

3.4 Optimal junction geometry

The optimal junction width and depth under different conditions is summarized in Table 3. The selection of optimal junction designs is based on the results presented in Figure 10 and the corresponding results for concentration of 1000 suns. The optimal width was selected based on two considerations: highest efficiency and minimum depth. The depth is minimized in order to reduce the amount of material, as well as for reduction in the contact trench width (which is proportional to the depth). All the results in Table 3 were computed with bulk doping of 10^{16} cm^{-3}.

	1 sun BSR=0 cm/s		1 sun BSR=1000 cm/s		1000 suns BSR=0 cm/s		1000 suns BSR=1000 cm/s	
FSR cm/s	*W*	*H*	*W*	*H*	*W*	*H*	*W*	*H*
10	>160	50-70	60-80	90-110	50-70	20-40	45-60	40-60
100	80-120	60-80	50-70	90-110	40-60	40-60	45-60	60-80

Table 3: Optimal junction width *W* [µm] and depth *H* [µm] for different values of illumination flux, FSR, and BSR

The most striking observations from the table are that: (1) the optimal junction geometry does not vary much over a wide range of parameters, and (2) the optimal

junction geometry is very different from the junctions presented and analyzed previously. The optimal junction width is 80 µm or less in most cases, compared to 250 µm in [2] and [11]. The optimal junction depth is 100 µm or less in most cases, compared to 500 µm in [2] and [11]. The junction width in [2] was based on the thickness of the wafers used for fabrication of the VMJ stack, and no optimization was reported. However, the optimization for 1 sun in [11] does report optimal junction width of about 200-250 µm. This contradiction may be explained by the fact that surface recombination was not considered in the model, and as shown here, this creates a strong tendency to reduce the optimal width. If the VMJ cell is fabricated by a monolithic process as assumed here, then the much narrower junctions needed for optimal operation can be considered.

The optimal VJ width and depth found in this study are affected by a significant aspect ratio related to the assumed fabrication method. The metallization trenches, which constitute inactive area and loss of incident radiation, are assumed to have a fixed trench aspect ratio, where the trench width is proportional to the junction depth. This leads to a reduction in efficiency of magnitude: $(H/20W)$. This should move the optimum junction design toward larger depth for a given width, or wider junctions for a given depth. In comparison, in [11] the loss of active area due to metallization is not dependent on depth, and therefore much higher junction depth can be considered.

4 Vertical multi junction module

In this chapter we consider a module made of VMJ cells under non-uniform concentrated illumination produced by a dish concentrator with a reflective homogenizer. The performance of this module, and in particular the loss attributed to electrical mismatch between the cells, is compared to the performance of a module made from conventional cells connected in series under the same incident radiation distribution.

4.1 Simulation setup

The simulation includes models of two components: the concentrator system and the PV dense array module. The optical part, shown in Figure 32, consists of a parabolic dish with a diameter of 0.96 m and focal length 0.48 m (corresponding to rim angle of 53.1°), and a square cross-section reflective homogenizer with variable length H and inlet aperture positioned at the focus of the dish. The PV module, shown in Figure 33, is positioned at the exit aperture of the homogenizer. The PV module is 4×4 cm and contains a dense array of VMJ cells connected in parallel. Each VMJ cell is made of *N* VJs connected internally in series. The spaces among the cells are neglected.

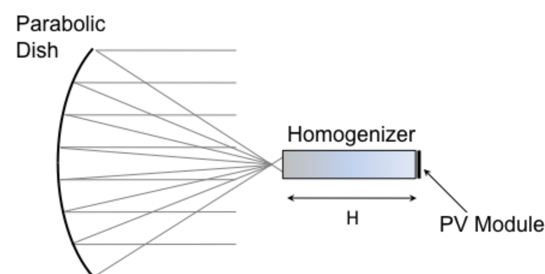
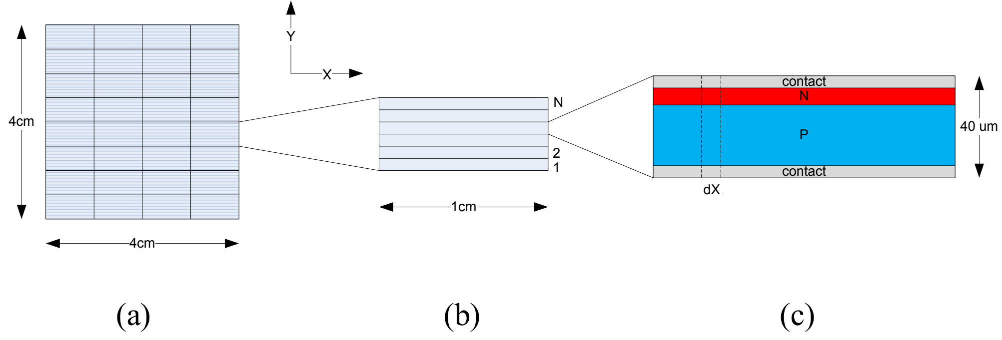


Figure 32: The optical concentrator system; H is the variable homogenizer length



(a) (b) (c)

Figure 33: (a) The module; (b) a VMJ cell made of *N* vertical junctions connected internally in series; (c) A single vertical junction and its segment of length dX

The module performance and the electrical mismatch loss were derived in two steps. First, the incident flux map at the module front plane was found using an optical simulation with the *OptiCAD* ray-tracing program. Next, the efficiency of the module was calculated for different values of *N*, the number of vertical junctions in each cell. This was repeated for several homogenizer lengths.

Figure 34 shows the incident flux concentration for different lengths of the homogenizer, including zero length (no homogenizer). The reflectivity of the homogenizer was taken to be 0.95. The homogenizer lengths were selected following [18]. In the simulation without a homogenizer, the module was placed 14.2 mm in front of the concentrator's focus. The optical efficiency of the homogenizers of different lengths as shown in Figure 34 are 98.9%, 98.18%, 97.28%, 95.52% respectively, and 98.4% without the homogenizer.

The performance of an individual vertical junction was based on a detailed simulation in the Synopsys Sentaurus TCAD program [21]. The semiconductor continuity and Poisson's equations were solved for a 40μm×1μm VJ. A single-diode equivalent circuit model was then generated by a fit to the I-V curve by using the well-known single diode equivalent circuit model:

$$I = I_{ph} - I_s\left[exp\left(\frac{q(V+IR_S)}{nKT}\right) - 1\right] - \frac{V+IR_S}{R_p} \tag{20}$$

Since the illumination on each vertical junction is not uniform, each vertical junction was divided into segments of length *dX* as shown in Figure 33c. For a small enough *dX* it can be assumed that the incident flux on each segment is uniform. The I-

V curve of the segment was generated based on the power incident on the segment, according to the distributions shown in Figure 34. The IV curve of the entire junction was then calculated from those of the segments, which are electrically connected in parallel (voltage matched). The IV curve of the entire VMJ cell with *N* junctions was then calculated by series connection of all junctions (current matched). The last step is the parallel connection (voltage matching) of all the VMJ cells in the module.

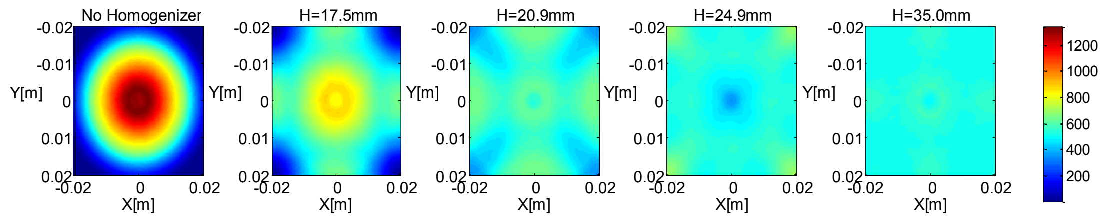
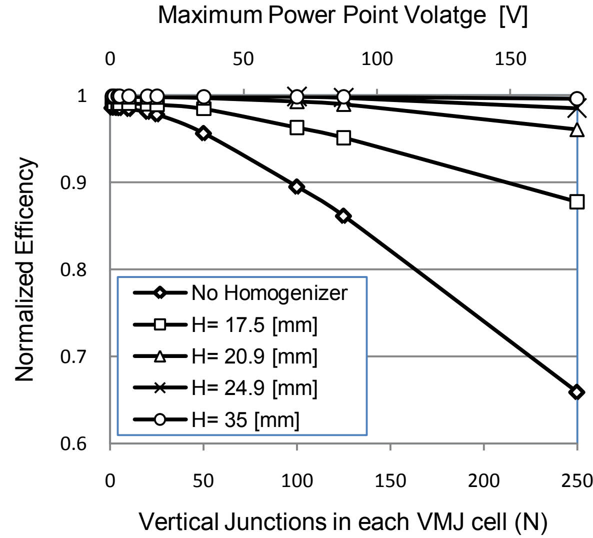


Figure 34: Incident concentration maps for different homogenizer length *H*

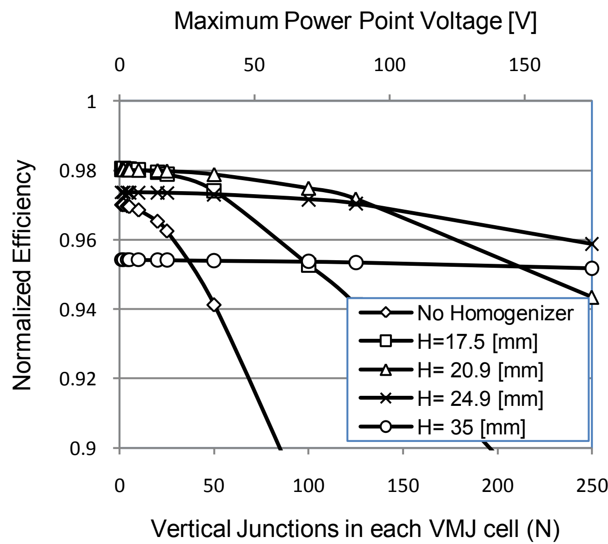
The performance of a reference module made from conventional cells connected in series was computed using an equivalent circuit model of each cell calculated for the average incident flux on each cell, and current matching all the cells in the module. The reference module comprised of 16 1×1 cm cells with the same characteristics as the vertical junction cells, except for their size and electrical connections.

4.2 Results

Figure 35(a) shows the normalized efficiency of the VMJ module: the module's calculated efficiency under the given incident flux distribution, divided by the hypothetical efficiency under a uniform irradiation distribution (no electrical mismatch) having the same total incident power. The reduction below a value of 1 is the mismatch loss. VMJ cell and module designs that produce a very small mismatch loss exist for all flux distributions, including the case of no homogenizer. As expected, the module's efficiency becomes less sensitive to the number of junctions connected in series as the input becomes more homogenous.



(a)



(b)

Figure 35: Normalized efficiency vs. number of vertical junctions in each cell, for different homogenizer lengths: (a) module mismatch losses only; (b) Module and homogenizer losses

Figure 35(b) shows the total receiver efficiency: the normalized module efficiency, multiplied by the homogenizer efficiency, which includes reflection losses and spillage around the homogenizer inlet aperture. The most uniform illumination does not necessarily produce the highest receiver efficiency due to the optical loss.

The selection of homogenizer length may be guided by the choice of desired module output voltage. For example, if an output voltage of 120 V is desired, the 24.9 mm homogenizer will yield the highest efficiency. For output voltage below 20 V the 17.5 mm homogenizer is best, but not using a homogenizer at all might be a better engineering choice with only a minor reduction in efficiency.

Figure 36 shows the efficiency achieved by modules with VMJ cells, with a fixed number of junctions in a cell of N=20 (module voltage about 14 V) for all homogenizer lengths, compared to the efficiency of the reference module with conventional cells connected in series under the same illumination. The VMJ module exhibits very low sensitivity to illumination non-uniformity, and maintains very high efficiency even without a homogenizer. The conventional module on the other hand shows high mismatch loss and a significant decrease in efficiency when the homogenizer length falls below 24 mm.

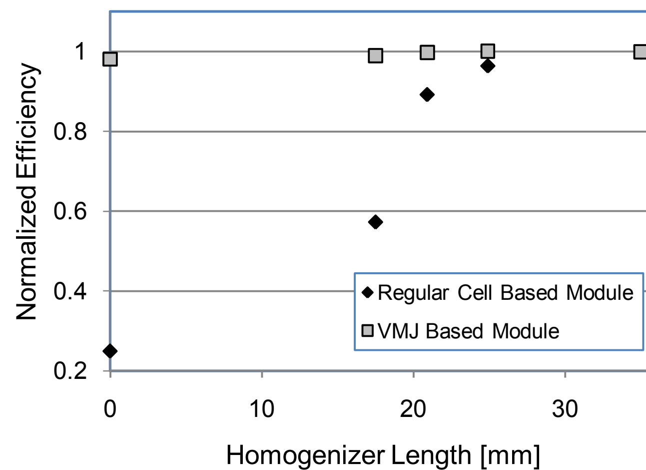


Figure 36: VMJ module and conventional module efficiencies vs. homogenizer length

The VMJ enable the use of shorter homogenizers, or even eliminating the homogenizer altogether. This reduces the optical losses and increases the overall efficiency compared to modules based on conventional cells connected in series and also can offer better performance under partly shading conditions. Furthermore, low sensitivity to VMJ cell size yields additional flexibility for optimization of the module's output voltage. High output voltage enable the use of a efficient DC/AC convertor

It must be noted here that since the model used through the calculations is based on Eq. 20, it does not model effects that occur at high negative voltages like diode brake-down. This is especially important for high values of N or cases where there is strong illumination gradient. In such cases, for low module voltages the working point of the least illuminated cells will be at very low voltages and such effects might occur.

When designing a module based on monolithic cells one must take several things into consideration. Under some illumination profiles there is peak efficiency for specific values of N. Yet, DC/AC inverters will usually have better efficiency for higher input voltages as already mentioned above. This tradeoff must be examined when choosing the right value for N. The second issue that should be considered is temperature effects. For high values of N, the illumination differences on a monolithic cell will be high and hot-spots might be formed. Obviously, it is impossible (and probably unwanted) to put a by-pass diode in parallel to each vertical junction. Hence, for high values of N high cell temperatures should be taken into consideration as well.

5 Vertical junction prototype

5.1. Fabrication

5.1.1 Substrate

We use a SOI wafer of N-type active area and SiO_2 isolation area (Figure 37). The SOI have SiO_2 area with thickness of $1\mu m$ and active area of $50\mu m$ using FZ technology with <100> surface direction.

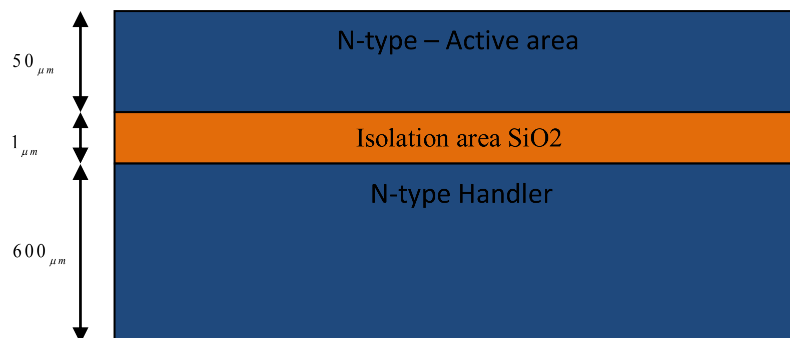


Figure 37: N-type SOI wafer with S_iO_2 isolation area

The fabrication process includes 4 stages:

5.1.2. Surface treatment and passivation

The surface treatment in our wafer consists of four elements:

- Roughening of wafer surface (Pyramids).
- First passivation layer of 55nm Si3N4.
- Second passivation layer of 55nm SiO2.
- Built in SiO2 in the SOI substrate is used as the RC.

Figure 38 illustrates the SOI scheme after surface treatment and passivation.

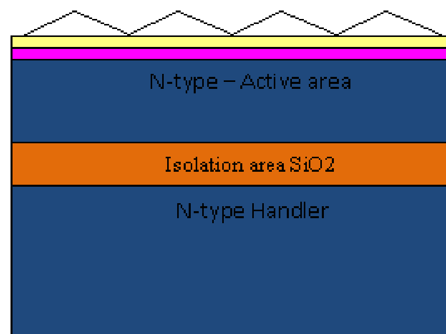


Figure 38: N-type SOI wafer with surface treatment and passivation

5.1.3. Trench fabrication

In order to fabricate the trench, a standard Deep Reactive Ion Etching (DRIE) process ($50\mu m$ deep) is used using a mask that we've designed.

DRIE is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers, with aspect ratios of 40:1 or more.

There are two main technologies for high-rate DRIE: cryogenic [22] and Bosch [23], the Bosch process is the only commercial production technique. Both technologies can fabricate 90° walls, but often the walls are slightly tapered.

The Bosch DRIE process involves alternate etching and passivation cycles. Because of that and because of the spontaneous nature of the etch in fluorinated chemistries, structures fabricated using this technology exhibit unwanted characteristic such as:

- Scalloped sidewalls
- Sidewalls angle
- Leg effect

We checked those effects on the VJ using TCAD.

Scalloped sidewalls: Figure 39 illustrates how scalloped sidewalls look like. It is possible to minimize the depth of those scallops by varying the operation conditions during the process. By changing the ratio of the etching time and passivation time we

can minimize the scallops on the sidewall as mentioned above. The dimensions of the scallops were taken from [24].

(a) (b)

Figure 39: Structure of VJ with sidewalls scalloping. TCAD model (a); SEM image (b)

The scallop caused the VJ efficiency to decrease by less than 0.3%.

Sidewalls angle: Sometimes a sidewall angle is a byproduct of the Bosch process that can be caused by wrong calibration of the machine.

Figures 40 illustrate the sidewalls angle. The angles for the left side of the Figure are 92.66 deg and for the right side 87.44 deg. These angles were chosen because they are more than the average deviation of the machine which is ± 1 deg. The cell efficiency improved (in both cases) from a cell with 90 deg sidewalls in about 0.1%.

(a) **(b)**

Figure 40: The structure of the cell with sidewalls in an angle. Large ratio, 92.66 deg (a) Small ratio. 87.44 deg (b)

Leg effect: The leg effect happens when uneven trenches widths are placed in one wafer. Figure 41 illustrates the structure that was checked for the leg effect. The leg dimensions were taken based on typical DRIE results. The leg caused the VJ efficiency to decrease by less than 0.25%.

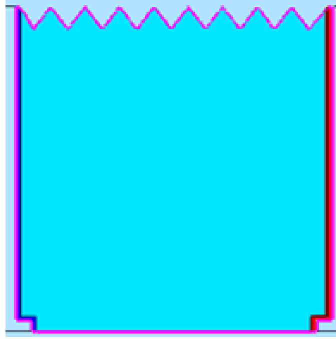


Figure 41: The structure of the cell with leg effect

We designed a mask which consists of a repeating array of junctions with the following widths: $40\mu m$, $45\mu m$, $50\mu m$, $55\mu m$, $60\mu m$, $75\mu m$, $100\mu m$, $150\mu m$, $200\mu m$, $250\mu m$ and $300\mu m$. The distance between two junctions is $600\mu m$. The wafer is coated by a photo-resist, exposed by the pattern of the mask and then the trenches are created by DRIE.

Figure 42 illustrates the SOI scheme after DRIE process.

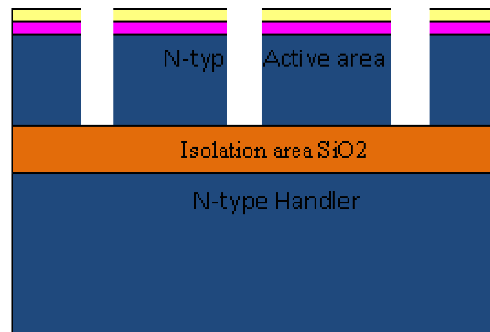


Figure 42: N-type SOI wafer with surface treatment, passivation and trenches

5.1.4. Doping process

Conventional doping methods (Ion implantation and diffusion) do not have the ability to control anisotropic doping (fixed width, vertical depth). However they do have control over isotropic doping, which spreads in all directions and this is contradictory to what is required in the case of the VJ (Figure 43).

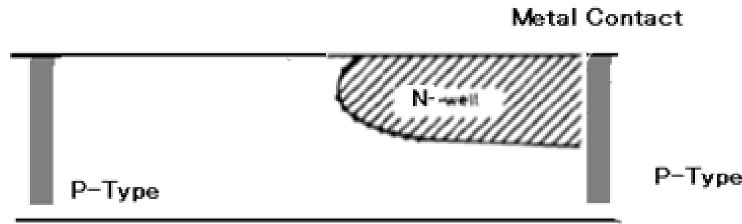


Figure 43: Isotropic Expansion of Diffusion

In general, it is difficult to get deep penetration when using ion implantation, since extremely high energy ions are required. As such, ion implantation is a surface modification technique and not suitable for changing the entire bulk property of a solid [25].

Therefore, an alternative approach is required, something that is not conventional and not too expensive.

Trench sidewall doping is a solution that we came up with. Among the various lateral devices emerging in recent years, most notable are both high power and high speed DRAM devices [26], the control of dopant implantation along silicon trench sidewalls and formation of trenches is a major issue for such devices. The concept is based on the utilization of conventional processing techniques under different operating conditions; the idea is to first create a high aspect-ratio trench, and then introduce the dopant through the sidewalls of the trench by means of ion implantation at very small angles θ, relative to the normal (Figure 44).

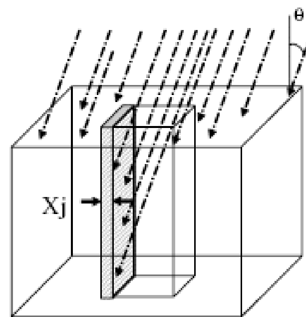


Figure 44: Schematic of Implantation in Trench Sidewall

This concept is very attractive and convenient for VJ, not only does it provide an answer to the VJ fabrication issue, but also it gives an added bonus of a trench that is

ready for metal contact deposition, for the purpose of connecting all the sub-cells in series, under monolithic conditions.

Implantation using angle in order to implant only one side wall is very "tricky". Our prototype consists of wide trenches so this shouldn't be a problem but if the trenches are going to be narrower, doping one side without affecting the other side is not trivial.

Figure 45 illustrates the SOI scheme after surface doping.

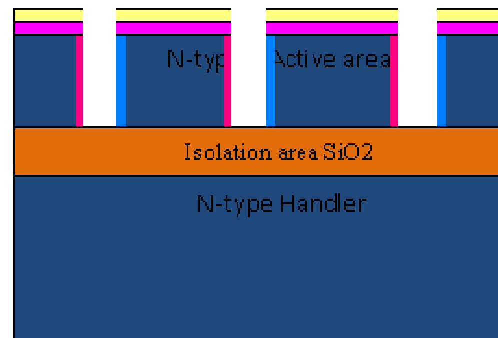


Figure 45: N-type SOI wafer with surface treatment, passivation, trenches and doping

5.1.5. Metal deposition

For the metal deposition, we use the PVD deposition method

Figure 46 illustrates the SOI scheme after surface PVD.

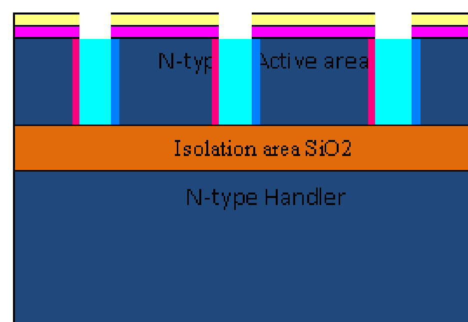


Figure 46: N-type SOI wafer with surface treatment, passivation, trenches, doping and metals

5.2 Setup of the I-V system

The measurement station comprises of 3 basic elements:

1. Sun simulator: We use a Cermax lamp combined with elliptical concentrator in order to get a collimated illumination.
2. Chip carrier and VJ chip:

Chip size: The chip will be comprised of 2 rows, each comprised of 11 VJs of varying widths (Section 5.1.3) electrically isolated from each other. Each row is 7.285mm wide and 5.1mm long. Hence the total chip size will be 7.285mm*10.2mm. A schematic of the chip is shown in Figure 47.

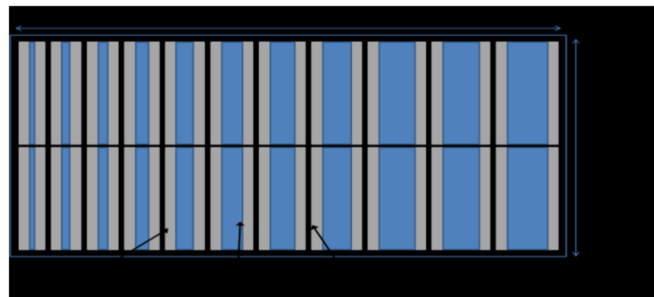


Figure 47: Chip schematic view

Electrical connections: Each VJ has two electrical connections. Since there is a total of 11 junctions in each row, 44 electrical pads are required. Since the wires should not shade the cells, the pads are located on the two opposite sides of the chip as shown in Figure 48. The wire bonding scheme between the VJs and the chip carrier is illustrated in Figure 49.

Heat dissipation: An external cooling device will be attached to the back surface of the carrier. Hence, the back surface of the carrier must be flat and the carrier should exhibit low heat resistance. The chip will be connected to the carrier using thermal pads.

Temperature measurement: Since the chip temperature is going to be measured using a thermocouple, groves should be made in the carrier in which the thermocouple wires will be placed.

In each measurement, just the measured junction (out of the 11 junctions on each chip) is illuminated. A metal cover is placed above the chip to shed the other

junctions. This step is done to prevent unwanted thermal effect, shunt effect and other fabrication defects effects that could occur due to the illumination of other series connected cells. To reduce such unknown effects even more, all the other junctions are also grounded.

X-Y stage: We are moving the cells and not the measurement unit. In that way, the sun simulator and the metal cover can stand in one place. The accuracy of the movement is about 1mm.

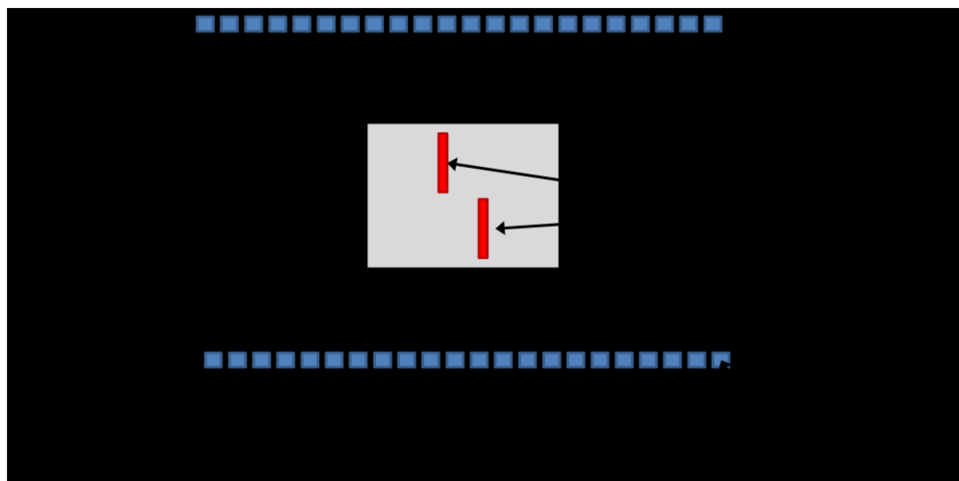


Figure 48**:** Chip Carrier schematic view

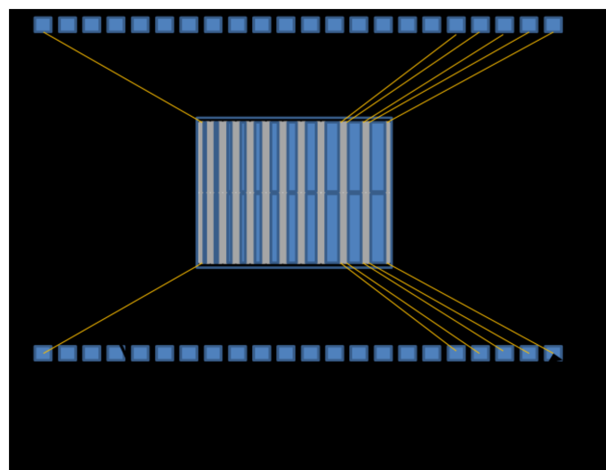


Figure 49**:** Chip and Chip Carrier electrical connections.

3. Source measure unit - we use Keithley Instruments Inc. measurement unit for the VJ chip I-V characterization.

6 Summary and Conclusions

In this work, we have presented a detailed analysis and optimization of a VJ Silicon solar cell under 1 to 2000 suns concentration, using a set of properties representing realistic wafer quality and fabrication processes, and a full 2-D model without major simplifying assumptions. The junction optimal design was found for different values of fabrication characteristics such as FSR, BSR and SRH lifetime. The results lead to the following main conclusions:

- The optimal junction dimensions are much smaller than the dimensions used in past VMJ cell tests and analyses.
- Conversion efficiency under high concentration can reach close to 30%, much higher than the 20% reported for past VMJ cells.
- In addition to the inherently low series resistance effect, an additional effect of photoconductivity is responsible for the outstanding performance of VMJ cells under high concentration.

The effect of photoconductivity under high concentration is an interesting ‘bonus’ of the VMJ structure, and has not been reported before. In conventional cells and Sliver cells, the photoconductivity effect will be negligible because the cell emitter is always heavily doped, making the increase in charge carriers concentration negligible.

The optimal junction geometry depends on the material quality and on the operating conditions (concentration). Nevertheless, width of 50 μm and depth of 60 μm would yield nearly optimal results for a broad range of realistic conditions and could be considered as the universal VJ geometry. Such a narrow width results in relatively high conversion efficiency even for very low SRH lifetime values.

Low series resistance and good performance under concentration have been reported in past VMJ cells of different junction dimensions, but the conversion efficiency of these VMJ cell was significantly lower. This indicates the need to optimize the junction dimensions, which are far from the optimum range that we have found. It may be difficult to produce VMJ cells with very narrow junctions using the wafer stacking process of [2], and therefore different fabrication methods should be considered, such as monolithic fabrication of the junctions and metallization on a single wafer. We have assumed a process based on fabricating deep trenches in a SOI

and doping to create the junctions through the sidewalls of the trenches. Since such a process is unconventional and complicated, its feasibility requires further investigation. Other processes may be considered as well as alternatives to produce the same geometry and junction structure.

Since the tradeoff between metallization and series resistance is not encountered in the VJ, the metallization area depends on the trench aspect ratio only. Hence, forming trenches with higher aspect ratio will result in a noticeable increase in cell efficiency. For example, trenches of aspect ratio of 1:40 will result in nearly 1% absolute increase in the VJ's efficiency. In the best case reported here, the efficiency would increase from about 29% to about 30% under 2000 suns.

In this work, we have shown the low sensitivity to non-uniform illumination for dense array CPV modules based on VMJ cells, enabling the use of shorter homogenizers, or even eliminating the homogenizer altogether. This reduces the optical losses and increases the overall efficiency compared to modules based on conventional cells connected in series. Furthermore, low sensitivity to VMJ cell size yields additional flexibility for optimization of the module's output voltage.

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7 Appendix

7.1 VJ voltage behavior

Consider two small elements of area dA_1 at some point near the top of the cell and dA_2 at another point near the bottom of the cell (Figure 50). These two small areas constitute two VJs connected together electrically in parallel through the SC.

The SC has low resistivity. Therefore, we can consider the two VJs to be connected in parallel. The voltage Voc_1 developed across dA_1 is much higher than the voltage Voc_2 developed across dA_2. It is clear from Figure 50 that the cell dA_2 will have a forward bias voltage of magnitude Voc_1-Voc_2 across it, and this will give rise to a hole current in the direction shown in Figure 50. If one can neglect the resistance of the circuit, this current will reduce the effective voltage across the cell dA1 to the value obtained across dA2. Thus, holes flow from the upper portions to the lower portions of the cell. The charges will quickly cross over to the other sides of the junction plane, giving rise to internal circulatory 'short-circuit currents'. These currents will reduce the voltage everywhere across the plane to the lowest value obtaining at dA_2.

J_{SC} unaltered by this effect. Voc at every point is reduced to zero in the short-circuit configuration. Hence, the potential gradient along the junction, which gives rise to the circulatory currents, disappears.

The energy wasted by the circulatory currents depends upon the load, being practically zero in the short-circuit case and a maximum in the open-circuit case.

The voltage and efficiency of the VJ increases if the total available light is not incident on one surface but divided equally, on the top and the bottom surfaces, such as in bifacial cells.

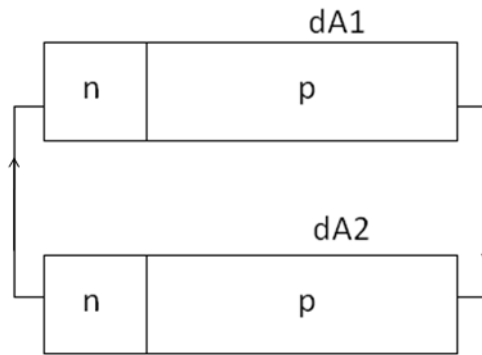

Figure 50: Flow of internal currents within the circuit of dA_1 and dA_2 connected in parallel, due to different intensities of illumination of the two junctions.

תקציר

לתא שמש המבוסס על צמתים אנכיים מסיליקון יש פוטנציאל לפעול בריכוזי קרינה גבוהים, בעיקר בשל התנגדות טורית נמוכה שנובעת מאופי התא – זרם נמוך ומתח גבוה. מדידות ואנליזות הראו עד כה נצילויות נמוכות של 20%.

עבודה זו מציגה חישובים מפורטים המראים כי יעילותם של התאים האנכיים יכולה להיות גדולה באופן משמעותי - קרוב ל-30% תחת ריכוז קרינה של 1000 שמשות ויותר. כדי להגיע ליעילות כזאת דרושה צומת אנכית בעלת מימדים גיאומטריים קטנים במידה משמעותית מהתאים האנכיים שהוצגו ויוצרו בעבר.

התאים האנכיים מצריכים גישת יצור שונה, בשיטה מונוליתית, במקום בהדבקה של מספר פיסות סיליקון האחד על השני. בנוסף, אנו מראים שהמרכיב העיקרי האחראי לביצועים הטובים של התא האנכי תחת ריכוז קרינה גבוה נובע מהגדלת הפוטו-מוליכות. גורם זה זניח בדרך כלל בתאי סיליקון סטנדרטיים אופקיים, אך במקרה של תאים אנכיים אפקט זה מונע את הגדלת ההתנגדות הטורית עם עליית ריכוז הקרינה ומוביל לעליה בנצילות התאים.

תאי שמש אנכים עם מתח יציאה גבוה מאפשרים חיבור מקבילי (התאמת מתח) במקום חיבור טורי (התאמת זרם), אשר מוביל להקטנת ההפסדים הנובעים מאי התאמה תחת תנאי קרינה לא הומוגניים.

ביצועים של מודול המורכב מתאים אנכיים תחת קרינה לא הומוגנית לא נלמד עד כה. עבודה זו מציגה את הביצועים של מודול המורכב מתאים אנכים מחוברים במקביל, בהשוואה למודול סטנדרטי שבו התאים מחוברים בטור. מספר הצמתים שמחוברים בטור בתוך כל תא אנכי הוא ערך משתנה ועליו נעשית האופטימיזציה.

התוצאות מראות יתרון מובהק למודול המורכב מתאים אנכיים לעומת מודול סטנדרטי תחת קרינה לא אחידה, מה שמאפשר הקטנת או אף הימנעות משימוש ברכיבים אופטיים המשמשים להומוגניזציה של הקרינה.

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